DATA SHEET

SAA7196
Digital video decoder, Scaler and Clock generator circuit (DESCPro)

Product specification
File under Integrated Circuits, IC22

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Digital video decoder, Scaler and Clock generator circuit (DESCPro)

SAA7196

CONTENTS

1 FEATURES

- Digital 8-bit luminance input [video (Y) or CVBS]
- Digital 8-bit chrominance input [CVBS or C from CVBS, Y/C, S-Video (S-VHS or Hi8)]
- Luminance and chrominance signal processing for main standards PAL, NTSC and SECAM
- Horizontal and vertical sync detection for all standards
- User programmable luminance peaking for aperture correction
- Compatible with memory-based features (line-locked clock, square pixel)
- Cross colour reduction by chrominance comb-filtering for NTSC or special cross-colour cancellation for SECAM
- UV signal delay lines for PAL to correct chrominance phase errors
- Square-pixel format with 768/640 active samples per line
- The bidirectional expansion port (YUV-bus) supports data rates of $780 \times f_H$ (NTSC) and $944 \times f_H$ (PAL, SECAM) in 4 : 2 : 2 format
- Brightness, contrast, hue and saturation controls for scaled outputs
- Down-scaling of video windows with 1023 active samples per line and 1023 active lines per frame to randomly sized windows
- 2D data processing for improved signal quality of scaled luminance data, especially for compression applications
- Chroma key (α-generation)
- YUV to RGB conversation including anti-gamma ROM tables for RGB
- 16-word output FIFO (32-bit words)
- Output configurable for 32-, 24- and 16-bit video data bus
- Scaled 16-bit 4 : 2 : 2 YUV output
- Scaled 15-bit RGB (5-5-5+α) and 24-bit (8-8-8+α) output
- Scaled 8-bit monochrome output
- Line increment, field sequence (odd/even, interlace/non-interlaced) and vertical reset control for easy memory interfacing
- Output of discontinuous data bursts of scaled video data or continuous data output with corresponding qualifier signals
- Real-time status information
- I^2C-bus control
- Only one crystal of 26.8 MHz required
- Clock generator on chip.

2 GENERAL DESCRIPTION

The CMOS circuit SAA7196, digital video decoder, scaler and clock generator (DESCPro), is a highly integrated circuit for DeskTop Video applications. It combines the functions of a digital multistandard decoder (SAA7191B), a digital video scaler (SAA7186) and a clock generator (SAA7197).

The decoder is based on the principle of line-locked clock decoding. It runs at square-pixel frequencies to achieve correct aspect ratio. Monitor controls are provided to ensure best display.

Four data ports are supported:

- Port CVBS7 to CVBS0 of input interface; used in Y/C mode (see Fig.1) to decode digitized luminance and chrominance signals (digitized in two external ADCs). In normal mode, only this input port is used and only one ADC is necessary (see Fig.4)
- Port CHR7 to CHR0 of input interface; used in Y/C mode (see Fig.1) to decode digitized luminance and chrominance signals (digitized in two external ADCs)
- 32-bit VRAM output port; interface to the video memory. It outputs the down-scaled video data; different formats and operation modes are supported by this circuit
- 16-bit expansion port; this is a bidirectional port. In general, it establishes the digital YUV as known from the SAA71x1 family of digital decoders. In addition, the expansion port is configurable to send data from the decoder unit or to accept external data for input into the scaler. In input mode the clock rate and/or the sync signals may be delivered by the external data source.

Decoder and scaler units can run at different clock rates. The decoder processing always operates with a Line Locked Clock (LLC). This clock is derived from the CVBS signal and is suited best for memory based video processing; the LLC clock is always present. The scaler clock may be driven by the LLC clock or by an external clock depending on the configuration of the expansion port.

The circuit is I²C-bus controlled. The I²C-bus interface is clocked by LLC to ensure proper control.
The I²C-bus control is identical to that of the SAA7194.
It is divided into two sections:

- Subaddress 00H to 1FH for the decoder part (Tables 16 and 17)
- Subaddress 20H to 3FH for the scaler part (Tables 29 and 30).

The programming of the subaddresses for the scaler part becomes effective at the first Vertical Sync (VS) pulse after a transmission.

3 QUICK REFERENCE DATA

Measured over full voltage and temperature ranges.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD(tot)}$	total supply current	–	180	280	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
f_{BCK}	input clock frequency	–	–	32	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7196H	QFP120	plastic quad flat package; 120 leads (lead length 1.95 mm); body 28 × 28 × 3.4 mm; high stand-of height	SOT349-1

5 BLOCK DIAGRAM

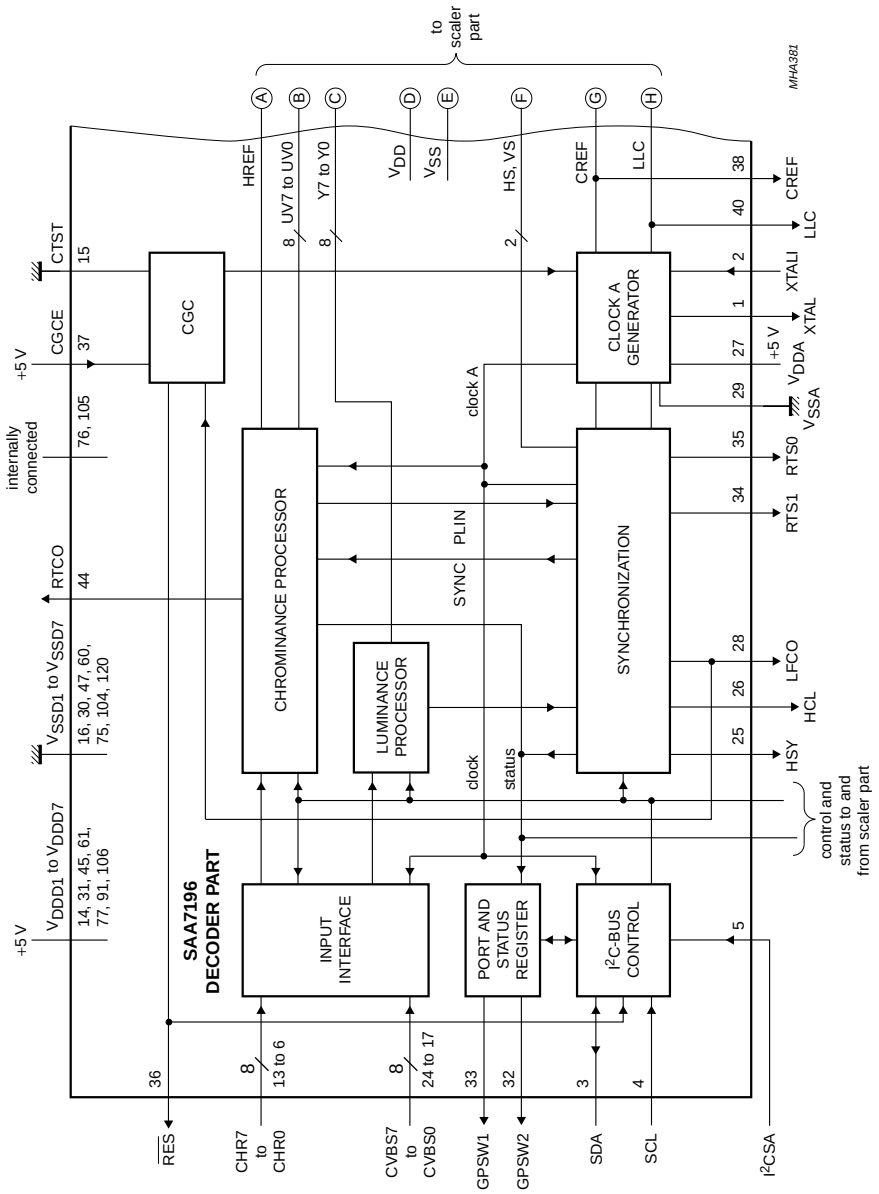


Fig.1 Block diagram of decoder part (continued in Fig.2).

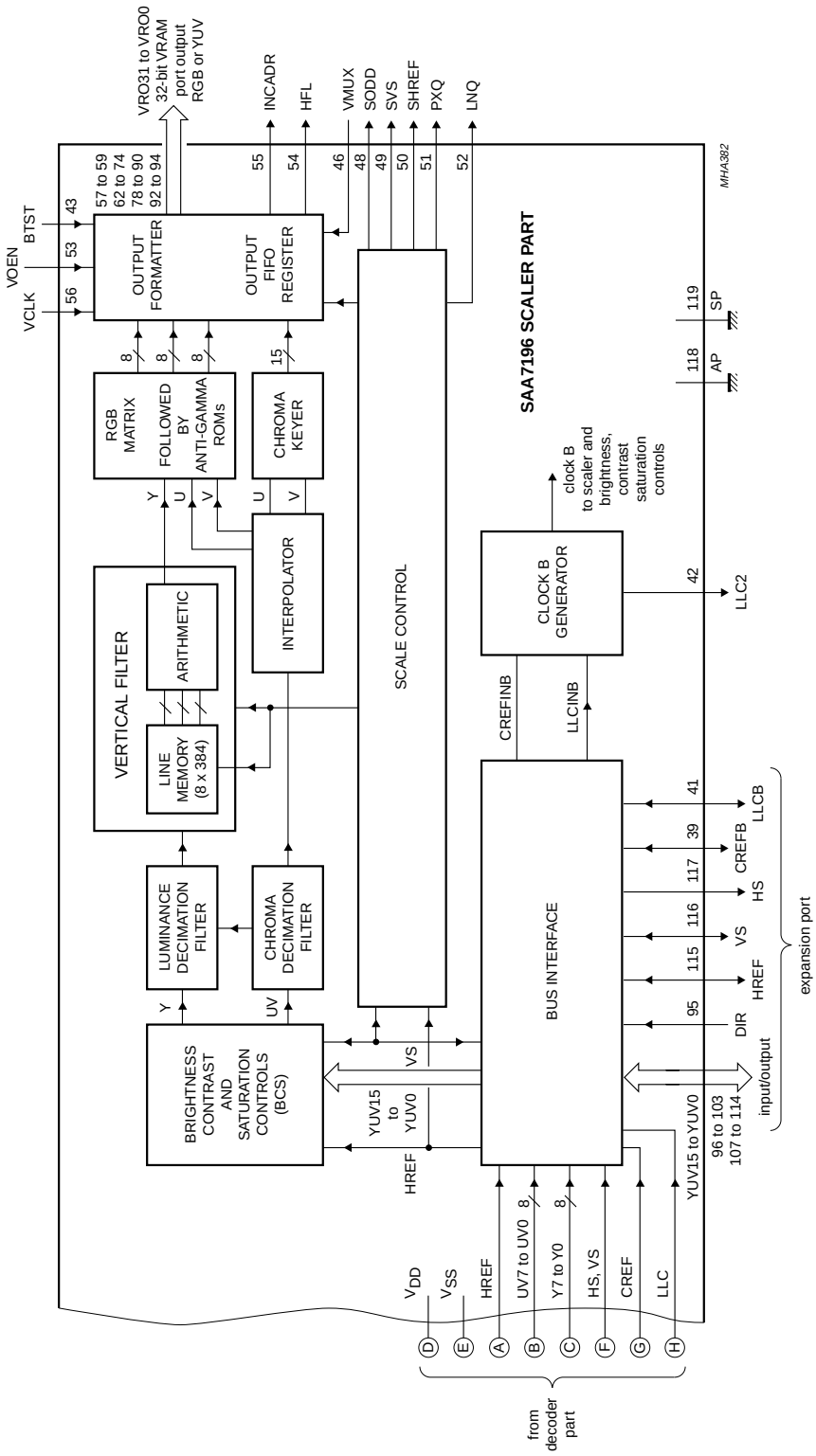


Fig.2 Block diagram of brightness, contrast, saturation controls and scaler part (continued from Fig.1).

6 PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
XTAL	1	O	26.8 MHz crystal oscillator output, not used if TTL clock signal is used
XTALI	2	I	26.8 MHz crystal oscillator input or external clock input (TTL, square wave)
SDA	3	I/O	I^2C-bus data line
SCL	4	I	I^2C-bus clock line
I^2CSA	5	I	I^2C-bus set address
CHR0	6	I	digital chrominance input signal (bit 0)
CHR1	7	I	digital chrominance input signal (bit 1)
CHR2	8	I	digital chrominance input signal (bit 2)
CHR3	9	I	digital chrominance input signal (bit 3)
CHR4	10	I	digital chrominance input signal (bit 4)
CHR5	11	I	digital chrominance input signal (bit 5)
CHR6	12	I	digital chrominance input signal (bit 6)
CHR7	13	I	digital chrominance input signal (bit 7)
V_{DDD1}	14	–	+5 V digital supply voltage 1
CTST	15	–	connected to ground (clock test pin)
V_{SSD1}	16	–	digital ground 1 (0 V)
CVBS0	17	I	digital CVBS input signal (bit 0)
CVBS1	18	I	digital CVBS input signal (bit 1)
CVBS2	19	I	digital CVBS input signal (bit 2)
CVBS3	20	I	digital CVBS input signal (bit 3)
CVBS4	21	I	digital CVBS input signal (bit 4)
CVBS5	22	I	digital CVBS input signal (bit 5)
CVBS6	23	I	digital CVBS input signal (bit 6)
CVBS7	24	I	digital CVBS input signal (bit 7)
HSY	25	O	horizontal sync indicator output (programmable)
HCL	26	O	horizontal clamping pulse output (programmable)
V_{DDA}	27	–	+5 V analog supply voltage
LFCO	28	O	line frequency control output signal to CGC (multiple of present line frequency)
V_{SSA}	29	–	analog ground (0 V)
V_{SSD2}	30	–	digital ground 2 (0 V)
V_{DDD2}	31	–	+5 V digital supply voltage 2
GPSW2	32	O	general purpose output 2 (controllable via I^2C-bus)
GPSW1	33	O	general purpose output 1 (controllable via I^2C-bus)
RTS1	34	O	real time status output 1; controlled by bit RTSE
RTS0	35	O	real time status output 0; controlled by bit RTSE
$\overline{RES}$	36	O	reset output, active LOW
CGCE	37	I	enable input for internal CGC (connected to +5 V)
CREF	38	O	clock qualifier output (test only)

SYMBOL	PIN	STATUS	DESCRIPTION
CREFB	39	I/O	clock reference qualifier input/output (HIGH indicates valid data on expansion port)
LLC	40	O	line-locked video system clock output, for front-end (ADCs) only; frequency: $1888 \times f_H$ for 50 Hz/625 lines per field systems and $1560 \times f_H$ for 60 Hz/525 lines per field systems
LLCB	41	I/O	line-locked clock signal input/output, maximum 32 MHz (twice of pixel rate in 4 : 2 : 2); frequency: $1888 \times f_H$ for 50 Hz/625 lines per field systems and $1560 \times f_H$ for 60 Hz/525 lines per field systems; or variable input clock up to 32 MHz in input mode
LLC2	42	O	line-locked clock signal output (pixel clock)
BTST	43	I	connected to ground; BTST = HIGH sets all outputs (except pins 1, 28, 38, 40 and 42) to high-impedance state (testing)
RTCO	44	O	real time control output
V_{DDD3}	45	–	+5 V digital supply voltage 3
VMUX	46	I	VRAM output multiplexing, control input for the 32- to 16-bit multiplexer (see Table 7)
V_{SSD3}	47	–	digital ground 3 (0 V)
SODD	48	O	odd/even field sequence reference output related to the scaler output (test only)
SVS	49	O	vertical sync signal related to the scaler output (test only)
SHREF	50	O	delayed HREF signal related to the scaler output (test only)
PXQ	51	O	pixel qualifier output signal to mark active pixels of a qualified line (polarity: bit QPP; test only)
LNQ	52	O	line qualifier output signal to mark active video phase (polarity: bit QPP; test only)
$\overline{VOE}$	53	I	enable input of VRAM output
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment/vertical reset control output
VCLK	56	I	clock input signal of FIFO output
VRO31	57	O	32-bit digital VRAM output port (bit 31)
VRO30	58	O	32-bit digital VRAM output port (bit 30)
VRO29	59	O	32-bit digital VRAM output port (bit 29)
V_{SSD4}	60	–	digital ground 4 (0 V)
V_{DDD4}	61	–	+5 V digital supply voltage 4
VRO28	62	O	32-bit VRAM output port (bit 28)
VRO27	63	O	32-bit VRAM output port (bit 27)
VRO26	64	O	32-bit VRAM output port (bit 26)
VRO25	65	O	32-bit VRAM output port (bit 25)
VRO24	66	O	32-bit VRAM output port (bit 24)
VRO23	67	O	32-bit VRAM output port (bit 23)
VRO22	68	O	32-bit VRAM output port (bit 22)
VRO21	69	O	32-bit VRAM output port (bit 21)
VRO20	70	O	32-bit VRAM output port (bit 20)

SYMBOL	PIN	STATUS	DESCRIPTION
VRO19	71	O	32-bit VRAM output port (bit 19)
VRO18	72	O	32-bit VRAM output port (bit 18)
VRO17	73	O	32-bit VRAM output port (bit 17)
VRO16	74	O	32-bit VRAM output port (bit 16)
V_{SSD5}	75	–	digital ground 5 (0 V)
i.c.	76	–	internally connected
V_{DDD5}	77	–	+5 V digital supply voltage 5
VRO15	78	O	32-bit VRAM output port (bit 15)
VRO14	79	O	32-bit VRAM output port (bit 14)
VRO13	80	O	32-bit VRAM output port (bit 13)
VRO12	81	O	32-bit VRAM output port (bit 12)
VRO11	82	O	32-bit VRAM output port (bit 11)
VRO10	83	O	32-bit VRAM output port (bit 10)
VRO9	84	O	32-bit VRAM output port (bit 9)
VRO8	85	O	32-bit VRAM output port (bit 8)
VRO7	86	O	32-bit VRAM output port (bit 7)
VRO6	87	O	32-bit VRAM output port (bit 6)
VRO5	88	O	32-bit VRAM output port (bit 5)
VRO4	89	O	32-bit VRAM output port (bit 4)
VRO3	90	O	32-bit VRAM output port (bit 3)
V_{DDD6}	91	–	+5 V digital supply voltage 6
VRO2	92	O	32-bit VRAM output port (bit 2)
VRO1	93	O	32-bit VRAM output port (bit 1)
VRO0	94	O	32-bit VRAM output port (bit 0)
DIR	95	I	direction control of expansion bus
YUV15	96	I/O	digital 16-bit video input/output signal (bit 15); luminance (Y)
YUV14	97	I/O	digital 16-bit video input/output signal (bit 14); luminance (Y)
YUV13	98	I/O	digital 16-bit video input/output signal (bit 13); luminance (Y)
YUV12	99	I/O	digital 16-bit video input/output signal (bit 12); luminance (Y)
YUV11	100	I/O	digital 16-bit video input/output signal (bit 11); luminance (Y)
YUV10	101	I/O	digital 16-bit video input/output signal (bit 10); luminance (Y)
YUV9	102	I/O	digital 16-bit video input/output signal (bit 9); luminance (Y)
YUV8	103	I/O	digital 16-bit video input/output signal (bit 8); luminance (Y)
V_{SSD6}	104	–	digital ground 6 (0 V)
i.c.	105	–	internally connected
V_{DDD7}	106	–	+5 V digital supply voltage 7
YUV7	107	I/O	digital 16-bit video input/output signal (bit 7); colour difference signals (UV)
YUV6	108	I/O	digital 16-bit video input/output signal (bit 6); colour difference signals (UV)
YUV5	109	I/O	digital 16-bit video input/output signal (bit 5); colour difference signals (UV)
YUV4	110	I/O	digital 16-bit video input/output signal (bit 4); colour difference signals (UV)
YUV3	111	I/O	digital 16-bit video input/output signal (bit 3); colour difference signals (UV)

SYMBOL	PIN	STATUS	DESCRIPTION
YUV2	112	I/O	digital 16-bit video input/output signal (bit 2); colour difference signals (UV)
YUV1	113	I/O	digital 16-bit video input/output signal (bit 1); colour difference signals (UV)
YUV0	114	I/O	digital 16-bit video input/output signal (bit 0); colour difference signals (UV)
HREF	115	I/O	horizontal reference signal
VS	116	I/O	vertical sync input/output signal with respect to the YUV input signal
HS	117	O	horizontal sync signal, programmable
AP	118	I	connected to ground (action pin for testing)
SP	119	I	connected to ground (shift pin for testing)
V_{SSD7}	120	–	digital ground 7 (0 V)

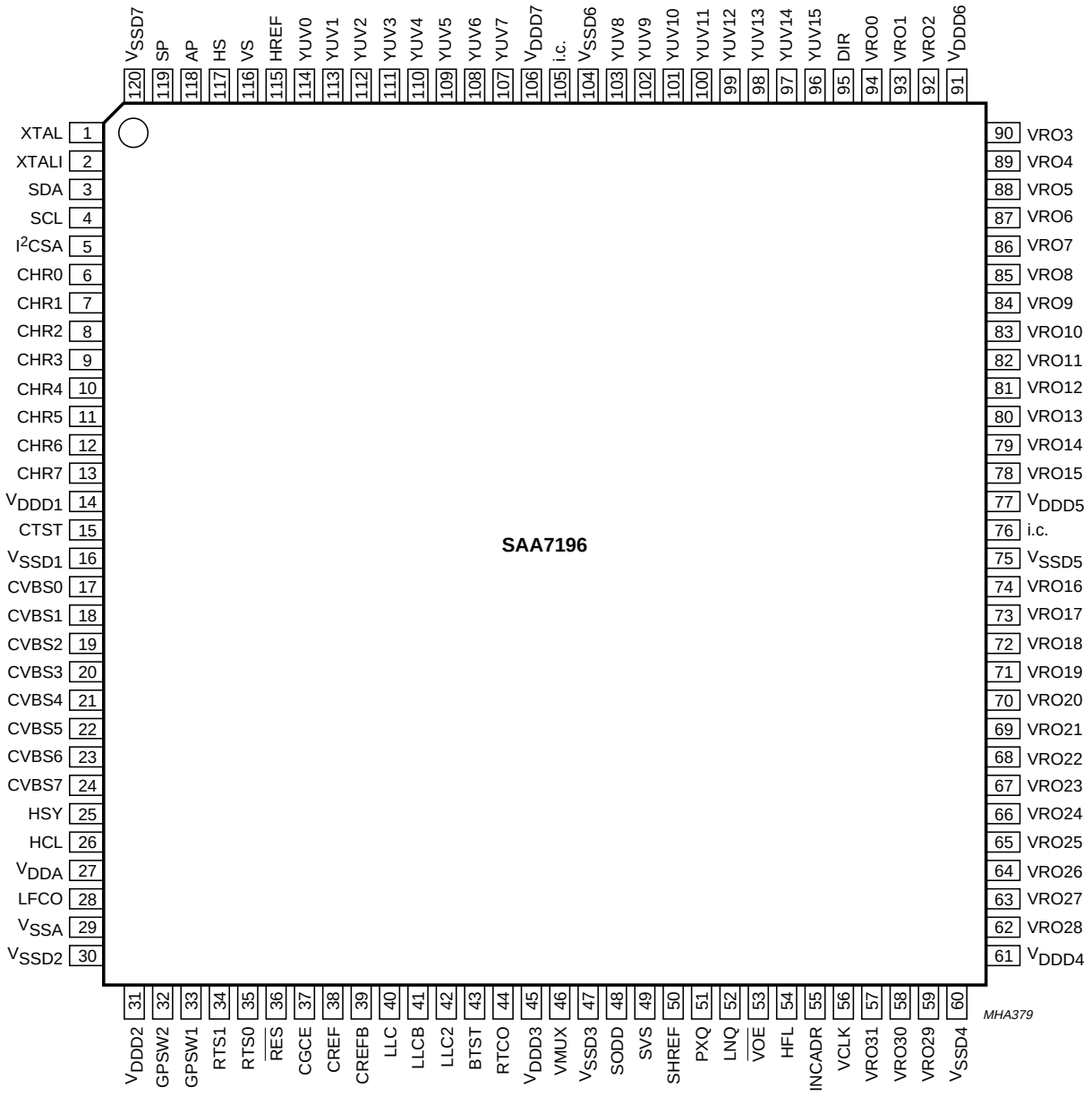


Fig.3 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Decoder part

PAL, NTSC and SECAM standard colour signals based on line-locked clock are decoded (see Fig.27). In Y/C mode, digitized luminance CVBS7 to CVBS0 and chrominance CHR7 to CHR0 signals (digitized in two external ADCs) are input. In normal mode only CVBS7 to CVBS0 is used. The data rate is 29.5 MHz (50 MHz systems) or 24.54 MHz (60 MHz systems).

7.1.1 CHROMINANCE PROCESSOR

The input signal passes the input interface and the chrominance band-pass filter to eliminate DC components and is finally fed to the multiplicative inputs of a quadrature demodulator, where two subcarrier signals (0 and 90° phase-shifted) from a local digital oscillator (DTO1) are applied.

The frequency is dependent on the present colour standard. The signals are low-pass filtered and amplified in a gain-controlled amplifier. A final low-pass stage provides a correct bandwidth performance.

PAL signals are comb-filtered to eliminate crosstalk between the chrominance channels according to PAL standard requirements.

NTSC signals are comb-filtered to eliminate crosstalk from luminance to chrominance for vertical structures.

SECAM signals are fed through a cloche filter, a phase demodulator and a differentiator to achieve proportionality to the instantaneous frequency. The signals are de-multiplexed in the SECAM recombination stage after passing a de-emphasis stage to provide the two serially transmitted colour difference signals.

The PLL for quadrature demodulation is closed via the cloche filter (to improve noise performance), a phase demodulator, a burst gate accumulator, a loop filter PI1 and a discrete time oscillator DTO1. The gain control loop is closed via the cloche filter, amplitude detector, a burst gate accumulator and a loop filter PI2.

The sequence processor switches signals according to standards.

7.1.2 LUMINANCE PROCESSOR

The data rate of the input signal is reduced to LLC2 frequency by a sample rate converter in the input interface. The high frequency components are emphasized in a prefilter to compensate for losses in the succeeding chrominance trap. The chrominance trap is adjusted to a centre frequency of 3.58 MHz (NTSC) or 4.4 MHz (PAL, SECAM) to eliminate most of the colour carrier components. The chrominance trap is bypassed for S-VHS signals.

The high frequency components in the luminance signal are ‘peaked’ using a band-pass filter and a coring stage. The ‘peaked’ (high frequent) component is added to the ‘unpeaked’ signal part for sharpness improvement and output via variable delay to the expansion bus.

7.1.3 SYNCHRONIZATION

The sync input signal is reduced in bandwidth to 1 MHz before it is sliced and separated from the luminance signal. The sync pulses are compared in a detector with the divided clock signal of a counter. The resulting output signal is fed to a loop filter that accumulates all the phase deviations. Thereby, a discrete time oscillator DTO2 is driven generating the line frequency control signal LFCO. An external PLL generates the line-locked clock LLC from the signal LFCO. A noise-limited vertical deflection pulse is generated for vertical processing that also inserts artificial pulses if vertical input pulses are missing. 50/60 Hz as well as odd/even field is automatically detected by the identification stage.

7.2 Expansion port

The expansion port is a bidirectional interface for digital video signals YUV15 to YUV0 in 4 : 2 : 2 format (see Table 5). External video signals can be inserted to the scaler or decoded video signals of the decoder part can be output.

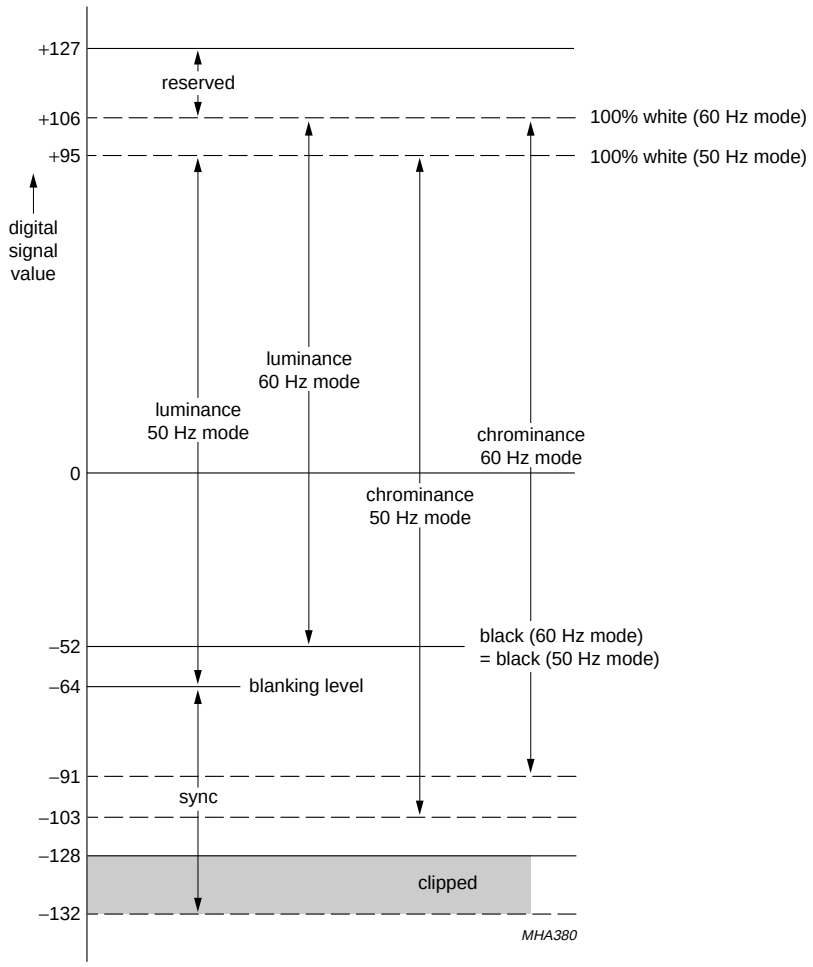
The data direction is controlled by pin 95 (DIR = HIGH: data from external; see Table 4).

YUV15 to YUV0, HREF, VS, LLCB and CREFB pins are inputs when bits OECL, OEHV, OEYC of subaddress 0E are set to ‘0’. Different modes are provided (for timing see Figs 6 to 8):

- Mode 0: all bidirectional terminals are outputs. The signal of the decoder part (internal YUV15 to YUV0) is switched to be scaled.
- Mode 1: external YUV15 to YUV0 is input to the scaler. LLCB/CREFB clock system and HREF/VS from the SAA7196 are used to control the external source. It is possible to switch between mode 0 and mode 1 by means of DIR input (see Fig.5).
- Mode 2: External YUV15 to YUV0 is input to the scaler. LLCB/ CREFB clock system and HREF/VS from external are used.

- Mode 3: YUV15 to YUV0 and HREF/VS terminals are inputs. External YUV15 to YUV0 is input to the scaler with HREF/VS reference from external. LLCB/CREFB clock system of the SAA7196 is used.

pixel wise switching of the scaler source is possible because the internal clock and sync sources are used.



All levels are related to EBU colour bar. Values in decimal at 100% luminance and 75% chrominance amplitude.

Fig.4 CVBS7 to CVBS0 input signal ranges.

7.3 Monitor controls BCS

7.3.1 Brightness and contrast controls

The luminance signal can be controlled via I²C-bus (see Table 16) by the bits BRIG7 to BRIG0 and CONT6 to CONT0.

Table 1 Brightness control

BRIGHTNESS CONTROL	VALUE
00H	minimum offset
80H	CCIR level
FFH	maximum offset

Table 2 Contrast control

CONTRAST CONTROL	VALUE
00H	luminance off
40H	CCIR level
7FH	1.9999 amplitude

7.3.2 Saturation control

The chrominance signal can be controlled via I²C-bus (see Table 16) by the bits SAT6 to SAT0 and HUE7 to HUE0.

Table 3 Saturation control

SATURATION CONTROL	VALUE
00H	colour off
40H	CCIR level
7FH	1.9999 amplitude

Clipping: all resulting output values are clipped to minimum (equals 1) and maximum (equals 254).

Table 4 Operation modes; notes 1 to 3

MODE	I²C BIT			DIR	INPUT SOURCE				
	OEYC	OEHV	OECL	PIN 95	YUV	HREF	VS	LLCB	CREFB
0	1	1	1	LOW	O	O	O	O	O
1	X	1	1	HIGH	I	O	O	O	O
2	X	0	0	HIGH	I	I	I	I	I
3	X	0	1	HIGH	I	I	I	O	O

Notes

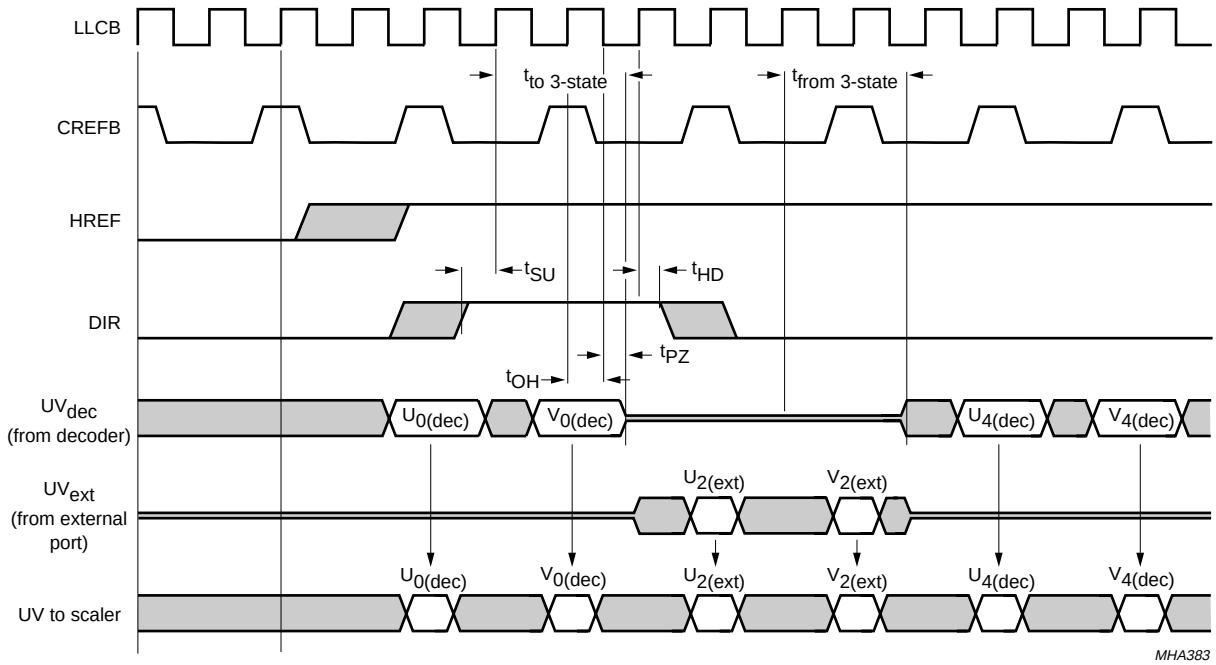
1. X = don't care.
2. I = input to monitor control/scaler.
3. O = output from decoder.

Table 5 YUV-bus format on expansion port; note 1

PIN	SIGNALS ON EXPANSION PORT (PIXEL BYTE SEQUENCE ON PINS) PIXEL ORDER				
	n	**n + 1**	**n + 2**	**n + 3**	**n + 4**
YUV15	Ye7	Yo7	Ye7	Yo7	Ye7
YUV14	Ye6	Yo6	Ye6	Yo6	Ye6
YUV13	Ye5	Yo5	Ye5	Yo5	Ye5
YUV12	Ye4	Yo4	Ye4	Yo4	Ye4
YUV11	Ye3	Yo3	Ye3	Yo3	Ye3
YUV10	Ye2	Yo2	Ye2	Yo2	Ye2
YUV9	Ye1	Yo1	Ye1	Yo1	Ye1
YUV8	Ye0	Yo0	Ye0	Yo0	Ye0
YUV7	Ue7	Ve7	Ue7	Ve7	Ue7
YUV6	Ue6	Ve6	Ue6	Ve6	Ue6
YUV5	Ue5	Ve5	Ue5	Ve5	Ue5
YUV4	Ue4	Ve4	Ue4	Ve4	Ue4
YUV3	Ue3	Ve3	Ue3	Ve3	Ue3
YUV2	Ue2	Ve2	Ue2	Ve2	Ue2
YUV1	Ue1	Ve1	Ue1	Ve1	Ue1
YUV0	Ue0	Ve0	Ue0	Ve0	Ue0

Note

1. e = even pixel number; o = odd pixel number.

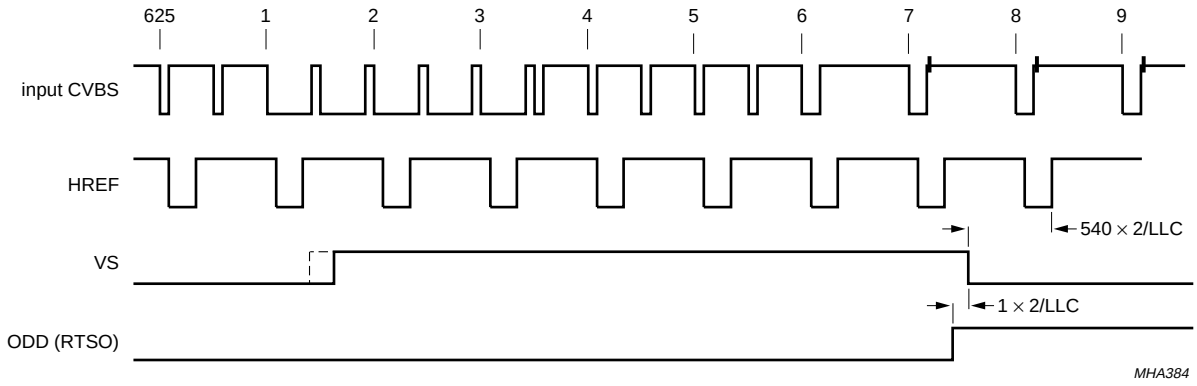


$t_{from\ 3\text{-}state(min)} = 1.5LLC + t_{PZ(min)}$

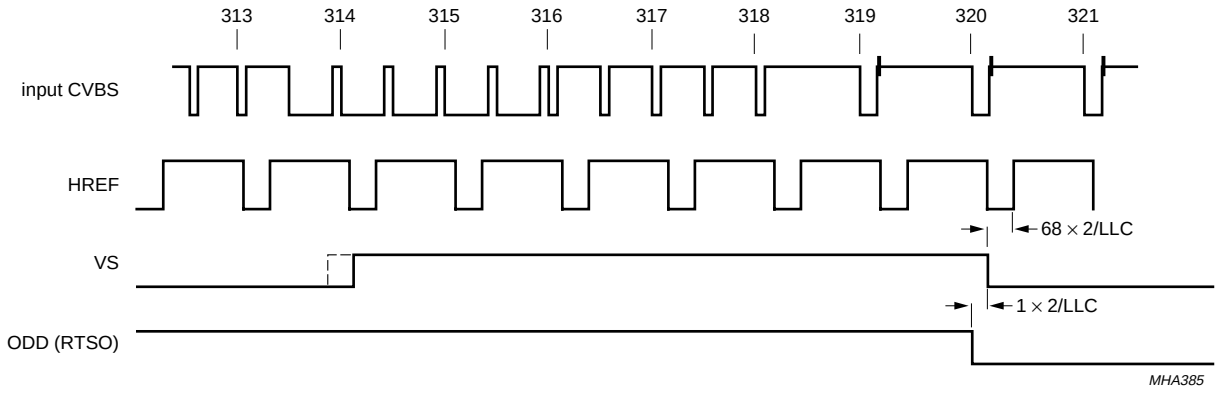
$t_{from\ 3\text{-}state} > t_{to\ 3\text{-}state}$

$t_{to\ 3\text{-}state(max)} = 1.5LLC + t_{PZ(max)}$

Fig.5 Real-time switching between mode 0 and mode 1 (internal/external YUV15 to YUV0).

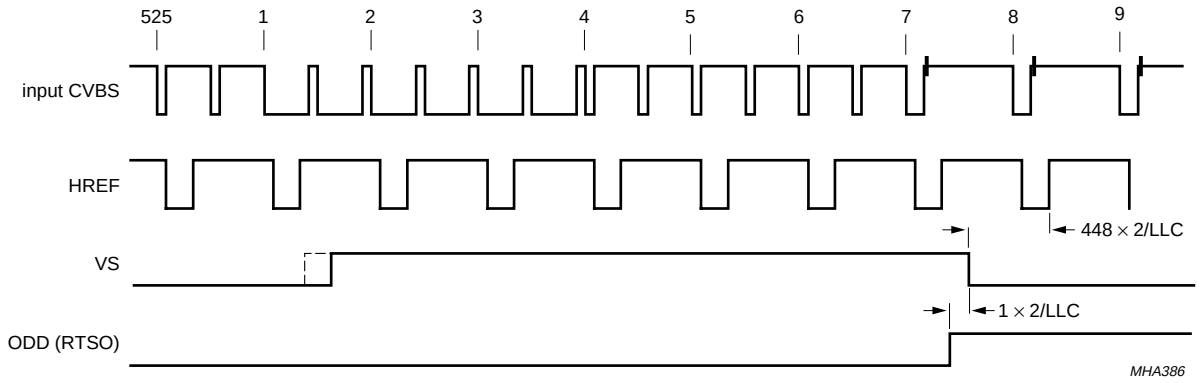


a. 1st field.

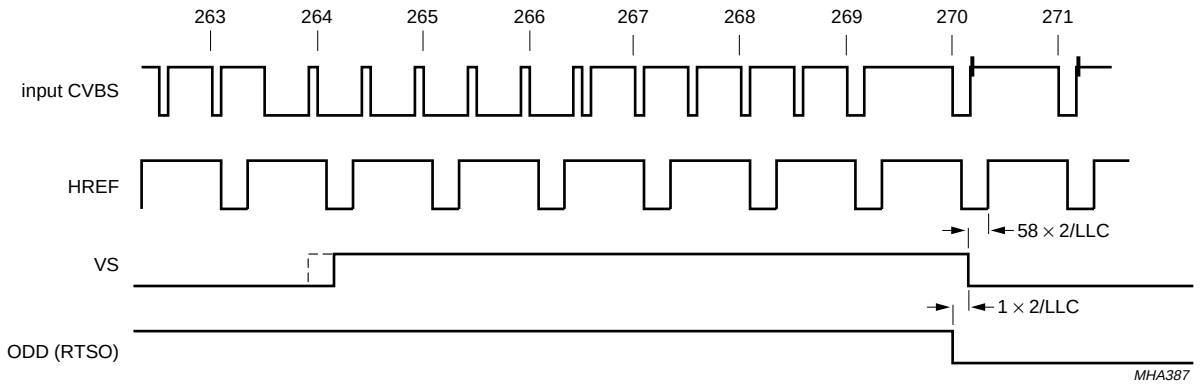


b. 2nd field

Fig.6 VS and ODD timing on expansion port (50 Hz).



a. 1st field.



b. 2nd field.

Fig.7 VS and ODD timing on expansion port (60 Hz).

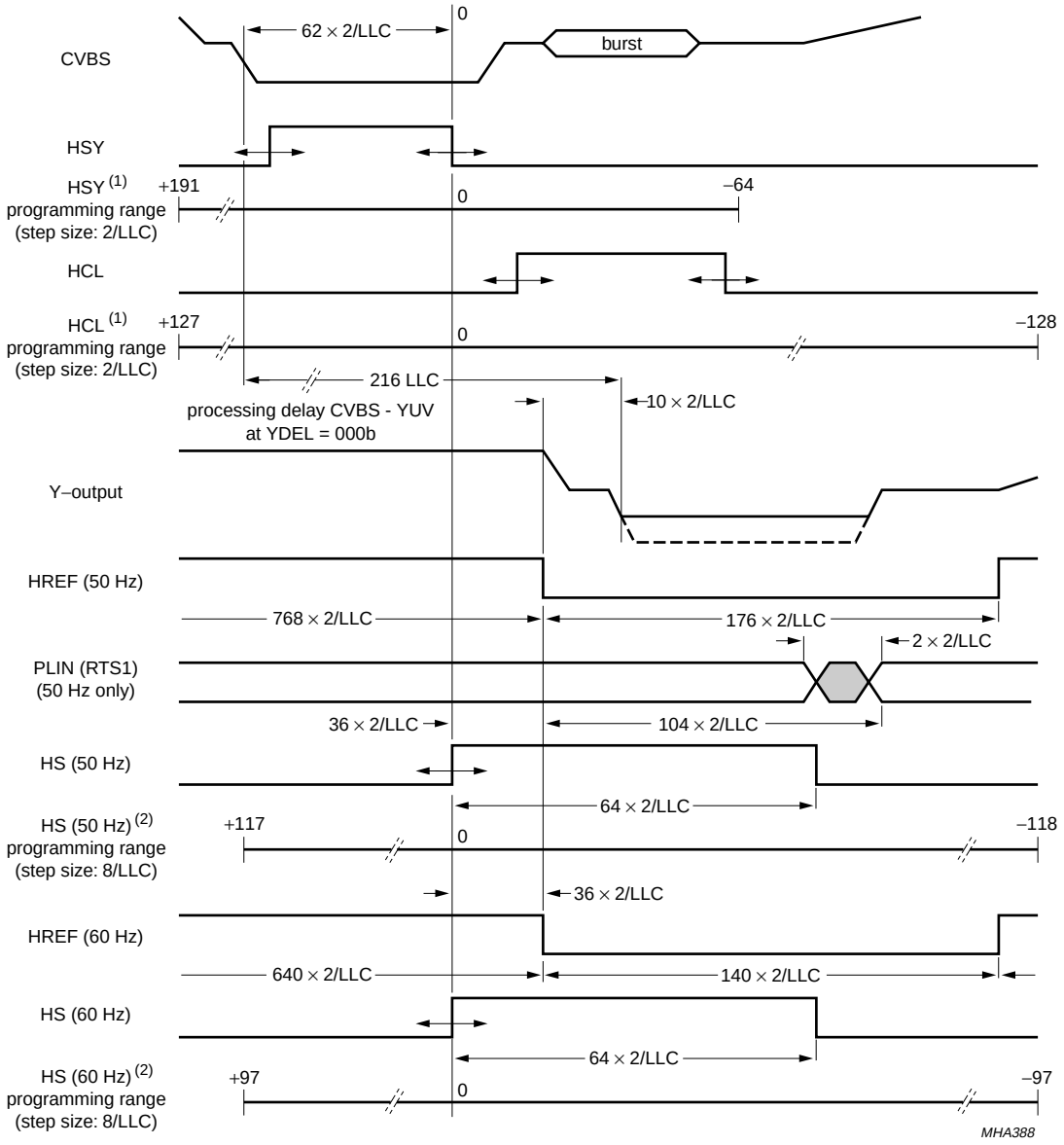


Fig.8 Horizontal sync timing at HRMV = 0 and HRFS = 0 (signals HSY, HCL, HREF, PLIN and HS; 50 and 60 Hz).

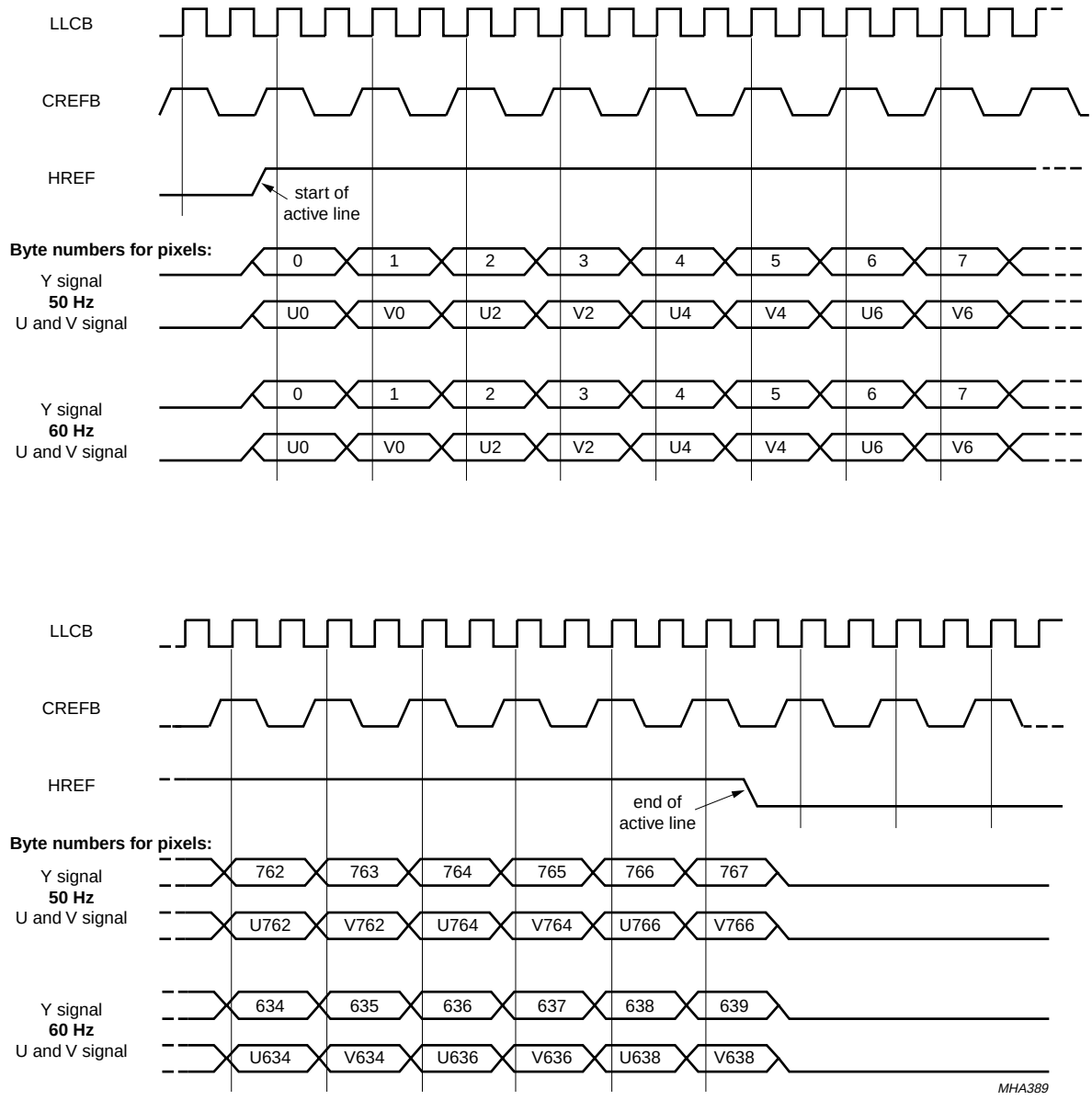
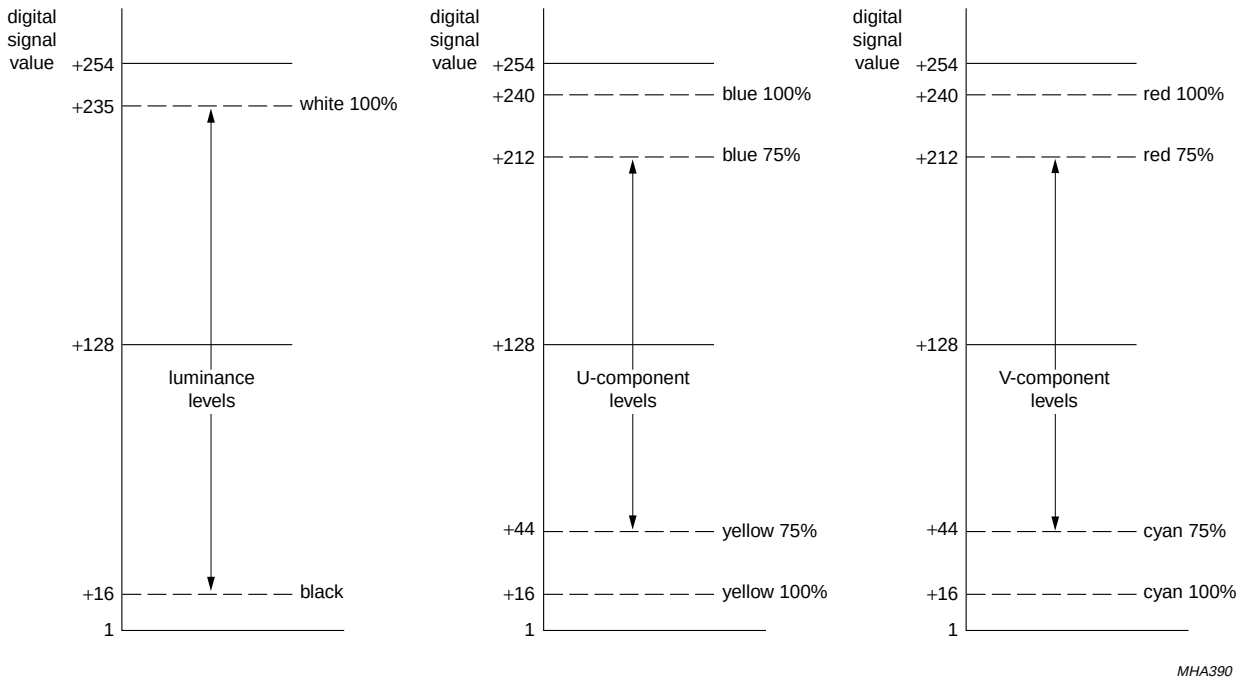


Fig.9 Horizontal and data multiplex timing on expansion port.



a. Y signal range. b. U signal range (B – Y). c. V signal range (R – Y).

Fig.10 Input and output signal levels on expansion port.

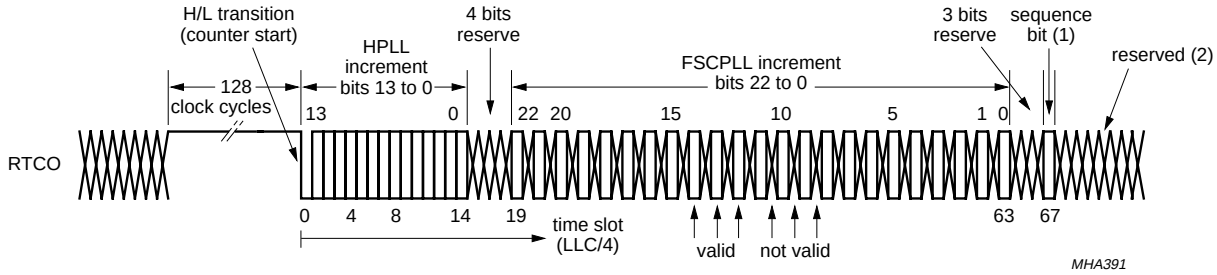
7.3.3 RTCO OUTPUT PIN 44

This real-time control and status output signal contains serial information about actual system clock, subcarrier frequency and PAL/SECAM sequence (see Fig.11). The signal can be used for various applications in external circuits, e.g. in a digital encoder to achieve ‘clean’ encoding.

7.3.4 RTS1 AND RTS0 OUTPUTS (PINS 34 AND 35)

These outputs can be configured in two modes dependent on bit RTSE (subaddress 0D):

- RTSE = 0: the output RTS0 contains the odd/even field identification bit (HIGH equals odd); output RTS1 contains the inverted PAL/SECAM sequence bit [HIGH equals non-inverted (R – Y)-line/DB-line]
- RTSE = 1: the output RTS0 contains the horizontal lock bit (HIGH equals PLL locked); output RTS1 contains the vertical detection bit (HIGH equals vertical sync detected).



(1) Sequence bit:
SECAM: 0 equals DB-line; 1 equals DR-line.
PAL: 0 equals (R – Y) line normal; 1 equals (R – Y) line inverted.
NTSC: 0 (no change).

(2) Reserve bits: 276 for 50 Hz systems; 188 for 60 Hz systems.

Fig.11 RTCO timing.

7.4 Scaler part

The scaler part receives YUV15 to YUV0 input data in 4 : 2 : 2 format.

The video data from the BCS control are processed in horizontal direction in two separate decimation filters. The luminance component is also processed in vertical direction (VPU_Y).

Chrominance data are interpolated to a 4 : 4 : 4 format; a chroma keying bit is generated. The 4 : 4 : 4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals. Uncorrected RGB and YUV signals can be bypassed.

A scale control unit generates reference and gate signals for scaling of the processed video data. After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word 32-bit output FIFO register. The scaling is performed by pixel and line dropping at the FIFO input. The FIFO output is directly connected to the VRAM output bus VRO31 to VRO0. Specific reference signals support an easy memory interfacing.

7.4.1 DECIMATION FILTERS

The decimation filters perform accurate horizontal filtering of the input data stream.

The signal bandwidth is matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced.

The signal bandwidth can be reduced in steps of (see Figs 29 and 30):

2-tap filter = –6 dB at 0.325 pixel rate

3-tap filter = –6 dB at 0.25 pixel rate

4-tap filter = –6 dB at 0.21 pixel rate

5-tap filter = –6 dB at 0.125 pixel rate

9-tap filter = –6 dB at 0.075 pixel rate.

The different characteristics are chosen independently by I^2C-bus control bits HF2 to HF0 when AFS = 0 (subaddress 28). In the adaptive mode with AFS = 1, the filter characteristics are chosen dependent on the defined sizing parameters (see Table 6).

7.4.2 VERTICAL PROCESSING (VPU_Y)

Luminance data is fed to a vertical filter consisting of a 384 × 8-bit RAM and an arithmetic block (see Fig.2). Subsampled and interpolation operations are applied. The luminance data is processed in vertical direction to preserve the video information for small scaling factors and to reduce artifacts caused by the dropping.
The available modes respectively transfer functions are selectable by bits VP1 and VP0 (subaddress 28). Adaptive modes, controlled by AFS and AFG bits (subaddresses 28 and 30) are also available (see Table 6).

Table 6 Adaptive filter selection (AFS = 1)

SCALING RATIO	FILTER FUNCTION(1)
XD/XS	horizontal
≤1	bypassed
≤14/15	filter 1
≤11/15	filter 6
≤7/15	filter 3
≤3/15	filter 4
YD/YS	vertical
≤1	bypassed
≤13/15	filter 1
≤4/15	filter 2

Note

1. See Chapter 8.

7.4.3 RGB MATRIX

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. Data is bypassed in 16-bit YUV formats or monochrome modes.

The matrix equations are these considering the digital quantization:

R = Y + 1.375 V

G = Y – 0.703125 V – 0.34375 U

B = Y + 1.734375 U.

7.4.3.1 Anti-gamma ROM tables

ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented. The tables can be used (bit RTB = 0, subaddress 20) to compensate gamma correction for linear data representation of RGB output data.

7.4.4 CHROMINANCE SIGNAL KEYER

The keyer generates an alpha signal to achieve a 5-5-5+α RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via I^2C-bus (subaddresses ‘2C to 2F’). A logic ‘1’ signal is generated if the amplitude is inside the specified amplitude range, otherwise a logic ‘0’ is generated.
Keying can be switched off by setting the lower limit higher than the upper limit (‘2C or 2E’ and ‘2D or 2F’).

7.4.5 SCALE CONTROL AND VERTICAL REGIONS

The scale control block SC includes address/sequence counters to define the current position in the input field and to address the internal VPU memories. To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register.

The scaling ratio in horizontal and vertical direction is estimated to control the decimation filter function and the vertical data processing in the adaptive mode (AFS and AFG bits). The input field can be divided into two vertical regions - the bypass region and the scaling region, which are defined via I^2C-bus by the parameters VS, VC, YO and YS.

7.4.5.1 Vertical bypass region

Data are not scaled and independent of I²C bits FS1 and FS0; the output format is always 8-bit gray scale (monochrome). The SAA7196 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active. This can be used, for example, to store video text information in the field memory. The start line of the bypass region is defined by the I²C bits VS; the number of lines to be bypassed is defined by VC.

7.4.5.2 Vertical scaling region

Data is scaled with start at line YO and the output format is selected when FS1 and FS0 are valid. This is the 'normal operation' area. The input/output screen dimensions in horizontal and vertical direction are defined by the parameters XO, XS and XD for horizontal and YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is shorter than XS, processing is aborted when the falling edge of HREF is detected. In this case the output line will have less than XD samples.

7.4.5.3 Vertical regions (see Fig.12)

- The two regions can be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region)
- The start of a normal active picture depends on video standard and has to be programmed to the correct value
- The offsets XO and YO have to be set according to the internal processing delays to ensure the complete number of destination pixels and lines (refer to Table 30)
- The scaling parameters can be used to perform a panning function over the video frame/field.

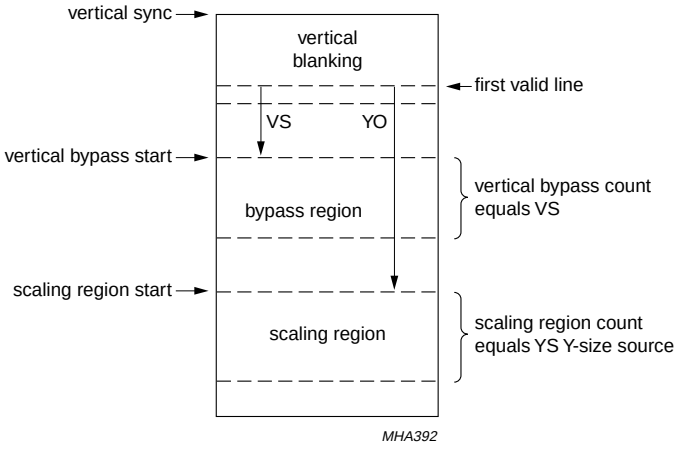


Fig.12 Vertical regions.

7.4.6 Output data representation and levels

Output data representation of the YUV data can be modified by bit MCT (subaddress 30). The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations; they are limited to the range of 1 to 254 in the 8-bit domain according to CCIR 601. In the event the YUV or monochrome luminance output formats are selected and bit LLV = 1, the luminance levels can be limited to:

- 16 (239) = black
- 235 (20) = white
- (...) = gray scale luminance levels.

For the 5-bit RGB formats a truncation from 8-bit to 5-bit word width is implemented. Fill values are inserted dependent on long word position and destination size (see Section 7.4.9):

- '1' for 24-bit RGB, Y and two's complement UV
- '128' for UV (straight binary)
- '254' in 8-bit gray scale format.

7.4.7 Output FIFO register and VRAM port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, VOF, FS1 and FS0. VRAM port formats are shown in Tables 7, 8 and 9. The FIFO register capacity is 16 words $\times$ 32-bit (for 32-, 24- or 16-bit video data).

The I^2C bits LW1 and LW0 can be used to define the position of the first pixel each line in the 32-bit long word format or to shift the UV sequence to VU in the 16-bit YUV formats. In case of YUV output, an odd pixel count XD results in an incomplete pair of UV data at the end (LW = 0) or beginning (LW = 2) of a line.

VRAM port inputs:

- VMUX, the VRAM output multiplexing signal
- VCLK to clock the FIFO register output data
- $\overline{VOE}$ to enable output data.

VRAM port outputs:

- HFL flag (half-full flag)
- INCADR (refer to Section 7.4.9)
- VRO31 to VRO0 VRAM port output data
- The reference signals for pixel and line selection on outputs VRO7 to VRO0 (only for 24- and 16-bit video data formats refer to Section 7.4.10).

7.4.8 VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchronously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchronously controlled by output reference signals on outputs VRO7 to VRO0 and a continuous VCLK of clock rate of $\frac{1}{2}$LLC (transparent data transfer with bit TTR = 1).

In general: the scaling capability of the SAA7196 can be used in various applications.

7.4.9 Data burst transfer mode

Data transfer on the VRAM port is asynchronously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided:

- HFL flag: the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH). By setting HFL = 1, the SAA7196 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit long word modes (16 LLC cycles for 16- and 24-bit modes). If there are pixels in the FIFO at the end of the line, which are not transferred, the circuit fills up the FIFO register with 'fill pixels' until it is half-full and sets the HFL flag to request a data burst transfer. After transfer is done, HFL is used in combination with INCADR to indicate the line increments (see Fig.13).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/non-interlaced or odd/even fields, see Figs 14 and 15) and control bits OF1 and OF0 (subaddress 20).
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (see Fig.13).
- $\overline{VOE}$ input enables output data VRO(n). The outputs are in 3-state mode at $\overline{VOE}$ = HIGH. $\overline{VOE}$ changes only when VCLK is LOW. If VCLK pulses are applied during $\overline{VOE}$ = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

It means:

HFL = 1 at the rising edge of INCADR: the ‘end of line’ is reached; request for line address increment

HFL = 0 at the rising edge of INCADR: the ‘end of field/frame’ is reached; request for line and pixel address reset.

7.4.10 TRANSPARENT DATA TRANSFER MODE

Data transfer on the VRAM port can be achieved synchronously (TTR = 1) controlled by output reference signals on outputs VRO7 to VRO0, and a continuous clock rate of ½LLC on input VCLK. The SAA7196 delivers a continuously processed data stream. Therefore, the extended formats of the VRAM output port are selected (bit EFE = 1; see Table 10).

The output signals VRO7 to VRO0 have to be used to buffer qualified preprocessed RGB or YUV video data. To avoid read/write collision at the internal FIFO, the VCLK timing and polarity must accord to the CREFB specification.
The YUV data is only valid in qualified time slots. Control output signals are (see Table 10 and Fig.16):

- α: keying signal of the chroma keyer
- O/E: odd/even field bit according to the internal field processing
- VGT: vertical gate signal, ‘1’ marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS
- HGT: horizontal gate signal, ‘1’ marks horizontal direction from XO to (XO + XS) lines, cut by HREF
- HRF: delay compensated horizontal reference signal
- LNQ: line qualifier signal, active polarity is defined by bit QPL
- PXQ: pixel qualifier signal, active polarity is defined by bit QPP.

7.4.10.4 VRAM port specifications

Table 7 VMUX control; note 1

BIT VOF	$\overline{\text{VOE}}$ (PIN 53)	VMUX (PIN 46)	VRAM BUS	
			VRO31 to VRO16	VRO15 to VRO0
0	0	0	3-state	active
0	0	1	active	3-state
1	0	X	active	active
X	1	X	3-state	3-state

Note

1. X = don’t care.

7.4.10.1 Interlaced processing (OF bits, subaddress 20)

To support correct interlaced data storage, the scaler delivers two INCADR/HFL sequences in each qualified line and an additional INCADR/HFL sequence after the vertical reset sequence at the beginning of an ODD field. Thereby, the scaled lines are automatically stored in the right sequence.

7.4.10.2 INCADR timing

The distance from the last half-full request (HFL) to the INCADR pulse may be longer than 64 × LLC. The state of HFL is defined for minimum 2 × LLC afterwards.

7.4.10.3 Monochrome format (see Table 10)

In case of TTR = 1 and EFE = 1 is Ya = Yb.

Table 8 VRAM port output data formats for bits 31 to 16 (continued in Table 9)

EFE-bit = 0 and VOF-bit = 1 (controllable via I^2C-bus); burst mode only; note 1.

PIXEL OUTPUT BIT	FS1 = 0; FS0 = 0 RGB 5-5-5+α 32-BIT WORDS			FS1 = 0; FS0 = 0 YUV 4 : 2 : 2 32-BIT WORDS			FS1 = 0; FS0 = 0 YUV 4 : 2 : 2 16-BIT WORDS			FS1 = 0; FS0 = 0 8-bit monochrome 32-BIT WORDS		
	n	n + 2	n + 4	n	n + 2	n + 4	n	n + 1	n + 2	n n + 1	n + 4 n + 5	n + 8 n + 9
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0

Note

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a, b, c, d = consecutive pixels.

Table 9 VRAM port output data formats for bits 15 to 0 (continued from Table 8)

EFE-bit = 0 and VOF-bit = 1 (controllable via I^2C-bus); burst mode only; note 1.

PIXEL OUTPUT BIT	FS1 = 0; FS0 = 0 RGB 5-5-5+α 32-BIT WORDS			FS1 = 0; FS0 = 0 YUV 4 : 2 : 2 32-BIT WORDS			FS1 = 0; FS0 = 0 YUV 4 : 2 : 2 16-BIT WORDS			FS1 = 0; FS0 = 0 8-bit monochrome 32-BIT WORDS		
	n + 1	n + 3	n + 5	n + 1	n + 3	n + 5	OUTPUTS NOT USED			n + 2 n + 3	n + 6 n + 7	n + 10 n + 11
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

Note

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a, b, c, d = consecutive pixels.

Table 10 VRAM port output data formats for bits 31 to 16 (continued in Table 11)

EFE-bit = 1 and VOF-bit = 1 (controllable via I^2C-bus); burst- and transparent- modes; notes 1 to 3.

PIXEL OUTPUT BIT	FS1 = 0; FS0 = 0 RGB 5-5-5+α(1) 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
	n	n + 1	n + 2	n	n + 1	n + 2	n	n + 1	n + 2	n n + 1	n + 2 n + 3	n + 4 n + 5
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ve7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ve6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ve5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ve4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ve3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ve2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ve1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ve0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0

Notes

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a and b = consecutive pixels; O/E = odd/even flag.
2. YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.
3. Data valid only when transparent mode active (bit TTR = 1) and VCLK pin connected to ½LLC clock rate.

Table 11 VRAM port output data formats for bits 15 to 0 (continued from Table 10)

EFE-bit = 1 and VOF-bit = 1 (controllable via I^2C-bus); burst- and transparent- modes; notes 1 to 3.

PIXEL OUTPUT BIT	FS1 = 0; FS0 = 0 RGB 5-5-5+α 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
	n	n + 1	n + 2	n	n + 1	n + 2	n	n + 1	n + 2	n n + 1	n + 2 n + 3	n + 4 n + 5
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7	α	α	α	α	X	α	α	α	α	α	α	α
VRO6	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

Notes

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a and b = consecutive pixels; O/E = odd/even flag.
2. YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.
3. Data valid only when transparent mode active (bit TTR = 1) and VCLK pin connected to ½LLC clock rate.

Table 12 VRAM port output formats for bits 31 to 16 (continued in Table 13)

EFE-bit = 0 and VOF-bit = 0 (controllable via I^2C-bus); burst mode only; note 1.

PIXEL OUTPUT BIT	VMUX											
	FS1 = 0; FS0 = 0 RGB 5-5-5+α 16-BIT LONG WORD				FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS				FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS			
	n		n + 2		n		n + 2		n n + 1		n + 4 n + 5	
	1	0	1	0	1	0	1	0	1	0	1	0
VRO31	α	Z	α	Z	Ye7	Z	Ye7	Z	Ya7	Z	Ya7	Z
VRO30	R4	Z	R4	Z	Ye6	Z	Ye6	Z	Ya6	Z	Ya6	Z
VRO29	R3	Z	R3	Z	Ye5	Z	Ye5	Z	Ya5	Z	Ya5	Z
VRO28	R2	Z	R2	Z	Ye4	Z	Ye4	Z	Ya4	Z	Ya4	Z
VRO27	R1	Z	R1	Z	Ye3	Z	Ye3	Z	Ya3	Z	Ya3	Z
VRO26	R0	Z	R0	Z	Ye2	Z	Ye2	Z	Ya2	Z	Ya2	Z
VRO25	G4	Z	G4	Z	Ye1	Z	Ye1	Z	Ya1	Z	Ya1	Z
VRO24	G3	Z	G3	Z	Ye0	Z	Ye0	Z	Ya0	Z	Ya0	Z
VRO23	G2	Z	G2	Z	Ue7	Z	Ue7	Z	Yb7	Z	Yb7	Z
VRO22	G1	Z	G1	Z	Ue6	Z	Ue6	Z	Yb6	Z	Yb6	Z
VRO21	G0	Z	G0	Z	Ue5	Z	Ue5	Z	Yb5	Z	Yb5	Z
VRO20	B4	Z	B4	Z	Ue4	Z	Ue4	Z	Yb4	Z	Yb4	Z
VRO19	B3	Z	B3	Z	Ue3	Z	Ue3	Z	Yb3	Z	Yb3	Z
VRO18	B2	Z	B2	Z	Ue2	Z	Ue2	Z	Yb2	Z	Yb2	Z
VRO17	B1	Z	B1	Z	Ue1	Z	Ue1	Z	Yb1	Z	Yb1	Z
VRO16	B0	Z	B0	Z	Ue0	Z	Ue0	Z	Yb0	Z	Yb0	Z

Note

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a, b, c, d = consecutive pixels; Z = high-impedance (3-state).

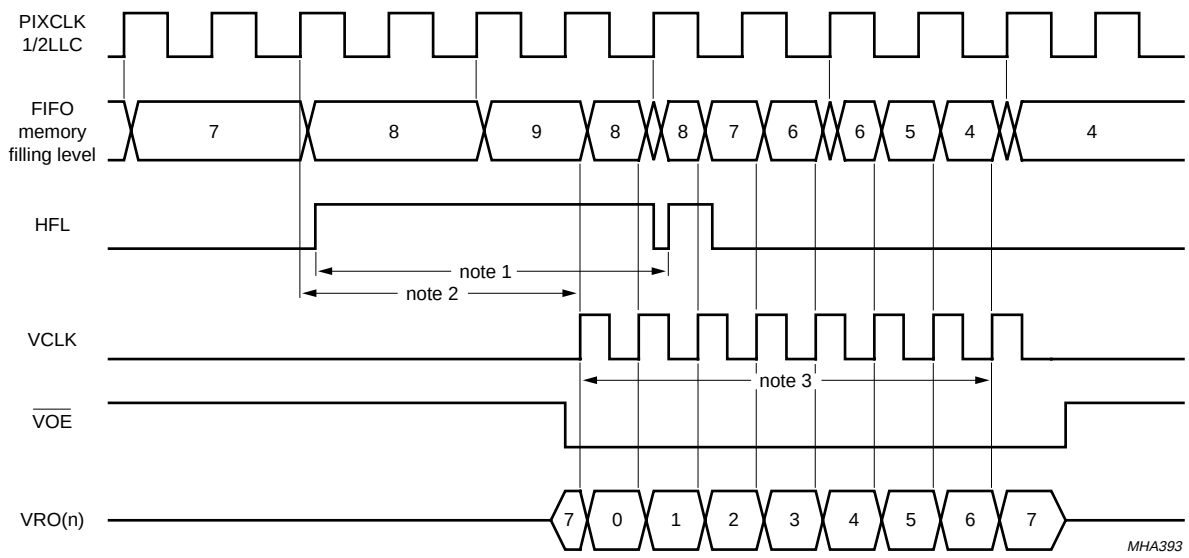
Table 13 VRAM port output data formats for bits 15 to 0 (continued from Table 12)

EFE-bit = 0 and VOF-bit = 0 (controllable via I^2C-bus); burst mode only; note 1.

PIXEL OUTPUT BIT	VMUX											
	FS1 = 0; FS0 = 0 RGB 5-5-5+α 16-BIT LONG WORD				FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS				FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS			
	n + 1		n + 3		n + 1		n + 3		n + 2 n + 3		n + 6 n + 7	
	1	0	1	0	1	0	1	0	1	0	1	0
VRO15	Z	α	Z	α	Z	Yo7	Z	Yo7	Z	Yc7	Z	Yc7
VRO14	Z	R4	Z	R4	Z	Yo6	Z	Yo6	Z	Yc6	Z	Yc6
VRO13	Z	R3	Z	R3	Z	Yo5	Z	Yo5	Z	Yc5	Z	Yc5
VRO12	Z	R2	Z	R2	Z	Yo4	Z	Yo4	Z	Yc4	Z	Yc4
VRO11	Z	R1	Z	R1	Z	Yo3	Z	Yo3	Z	Yc3	Z	Yc3
VRO10	Z	R0	Z	R0	Z	Yo2	Z	Yo2	Z	Yc2	Z	Yc2
VRO9	Z	G4	Z	G4	Z	Yo1	Z	Yo1	Z	Yc1	Z	Yc1
VRO8	Z	G3	Z	G3	Z	Yo0	Z	Yo0	Z	Yc0	Z	Yc0
VRO7	Z	G2	Z	G2	Z	Ve7	Z	Ve7	Z	Yd7	Z	Yd7
VRO6	Z	G1	Z	G1	Z	Ve6	Z	Ve6	Z	Yd6	Z	Yd6
VRO5	Z	G0	Z	G0	Z	Ve5	Z	Ve5	Z	Yd5	Z	Yd5
VRO4	Z	B4	Z	B4	Z	Ve4	Z	Ve4	Z	Yd4	Z	Yd4
VRO3	Z	B3	Z	B3	Z	Ve3	Z	Ve3	Z	Yd3	Z	Yd3
VRO2	Z	B2	Z	B2	Z	Ve2	Z	Ve2	Z	Yd2	Z	Yd2
VRO1	Z	B1	Z	B1	Z	Ve1	Z	Ve1	Z	Yd1	Z	Yd1
VRO0	Z	B0	Z	B0	Z	Ve0	Z	Ve0	Z	Yd0	Z	Yd0

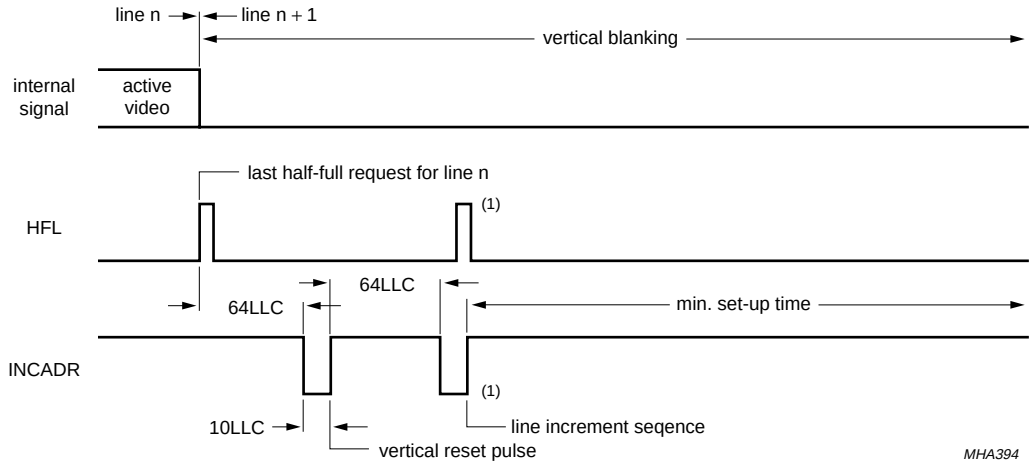
Note

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a, b, c, d = consecutive pixels; Z = high-impedance (3-state).



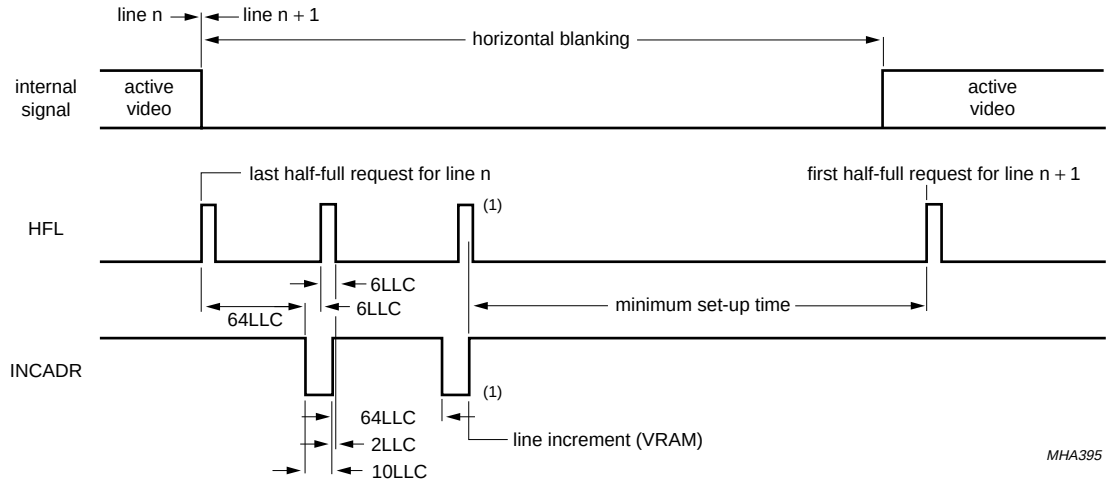
(1) Minimum 8 words available in FIFO.
(2) Maximum 32LLC (16PIXCLK).
(3) 1 transfer cycle (8 VCLK cycles).

Fig.13 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at $\overline{VOE}$ = HIGH, the FIFO register is unchanged, but the outputs VRO31 to VRO0 remain in 3-state position.



(1) Only available for interlaced processing at the beginning of an odd field.

Fig.14 Vertical reset timing to the VRAM.



(1) Pulse only at interlace scan.

Fig.15 Horizontal increment timing to the VRAM.

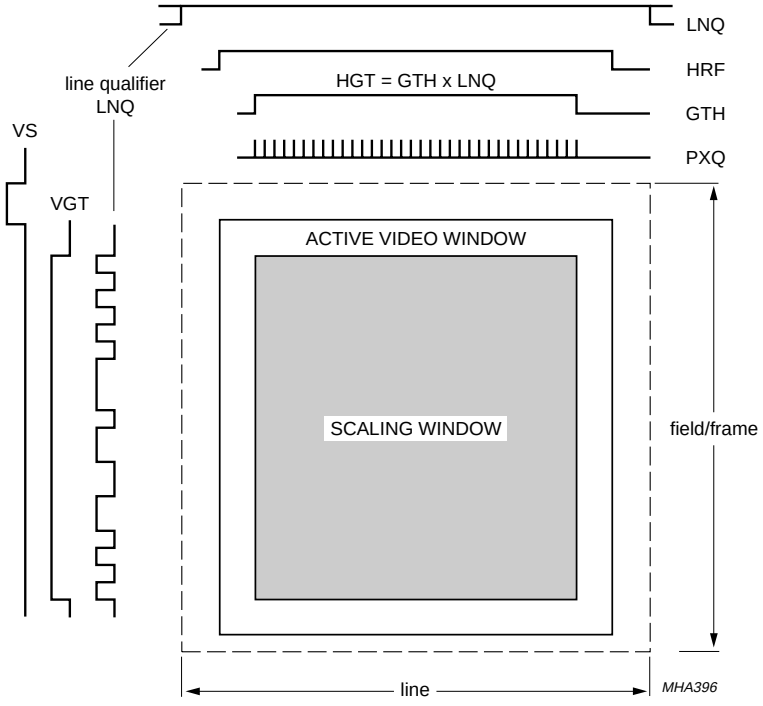


Fig.16 Reference signals for scaling window.

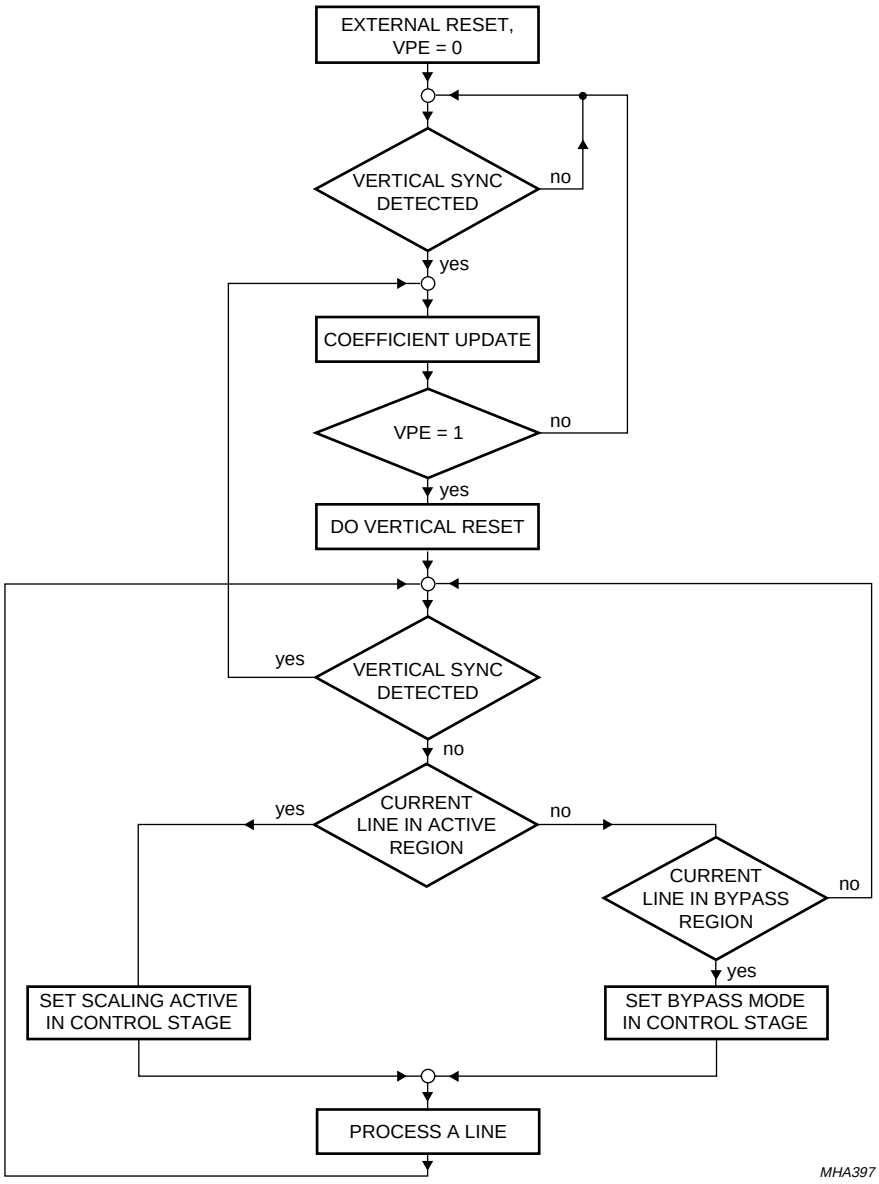


Fig.17 Operation cycle.

7.4.11 FIELD PROCESSING

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by bit OEF (see Table 14). Bit OEF can be stable 0 or 1 for non-interlaced input frames or non-standard input signals VS and/or HREF (nominal condition for VS and HREF; SAA7196 with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable bit OEF. Bit POE (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag and to compensate mis-detections. Thus, the SAA7196 can be used under various VS/HREF timing conditions.

The SAA7196 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. Bits OF1 and OF0 (see Table 30) determine the INCADR/HFL generation in 'data burst transfer mode'. One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage (see section 7.4.10.1).

7.4.12 OPERATION CYCLE

The operation is synchronized by the input field. The cycle is specified in the flow chart (see Fig.17).

The circuit is inactive after power-on reset, VPE = 0 and the FIFO control is set 'empty'. The internal control registers are updated with the falling edge of the VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the scaler waits for the beginning of a scaling or bypass region. If the active scaling region begins, while the bypass region is active, the bypass region is interrupted. If a vertical sync appears, the processing of the current line is finished. Then, the scaler performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed. The end of a line is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

The scaler part will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed.

After each line/field, the FIFO control is set to empty when the increment/vertical reset pulses are transmitted. No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle over-/underflow of the FIFO register.

7.5 Power-on reset

Power-on reset is activated at power-on or when the supply voltage decreases below 3.5 V. The indicator output $\overline{RES}$ is LOW for a time. The $\overline{RES}$ signal can be applied to reset other circuits of the digital TV system.

- Bits VTRC and SSTB in subaddress '0DH' are set to zero
- All bits in subaddress '0EH' are set to zero
- The FIFO register contents are undefined
- Outputs VRO, YUV, CREFB, LLCB, HREF, HS and VS are set to 3-state
- Output INCADR = HIGH
- Output HFL = LOW until bit VPE is set to '1'
- Subaddress '30' is set to 00H and bit VPE in subaddress '20H' is set to zero (see Table 29).

8 PROGRAMMING MODEL

8.1 I²C-bus format

S[1]	SLAVE ADDRESS[2]	A[3]	SUBADDRESS[4]	A[3]	DATA0[5]	A[3]		DATAn[5]	A[3]	P[6]

Notes

1. START condition.
2. 0100 000X (I^2CSA = LOW) or 0100 001X (I^2CSA = HIGH); X = read/write control bit [X = 0: order to write (the circuit is slave receiver); X = 1: order to read (the circuit is slave transmitter)].
3. Acknowledge, generated by the slave.
4. Subaddress byte (see Tables 16 to 30); if more than 1 byte data is transmitted, auto-increment of the subaddress is performed.
5. DATA byte (see Tables 16 to 30).
6. STOP condition.

8.2 I²C-bus status information

Table 14 I²C-bus status byte (X in address byte = 1; 41H at I²CSA = LOW or 43H at I²CSA = HIGH); see Table 15

FUNCTION	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Status byte 0 (transmitted after $\overline{RES}$ = 0 or at SSTB = 0)	ID3	ID2	ID1	ID0	DIR	X	OEF	SVP
Status byte 1 (transmitted at SSTB = 1)	STTC	HLCK	FIDT	X	X	X	ALTD	CODE

Table 15 Function of status bits; note 1

BIT	FUNCTION
DIR	state of input DIR (pin 95): direction control of expansion port YUV DIR = 0: the scaler uses internal source (decoder output) DIR = 1: the scaler uses external data of expansion bus
OEF	identification of field sequence dependent on HREF and VS 0 = even field detected 1 = odd field detected
SVP	state of VRAM port (state of, bit VPE cleared by $\overline{RES}$) 0 = inputs HFL and INCADR inactive 1 = inputs HFL and INCADR active
STTC	horizontal time constant information (for future application with logical comb-filter only) 0 = TV time constant (slow) 1 = VCR time constant (fast)
HLCK	horizontal PLL information 0 = HPLL locked 1 = HPLL unlocked
FIDT	field information 0 = 50 Hz system detected 1 = 60 Hz system detected
ALTD	line alternation 0 = no line alternating colour burst detected 1 = line alternating colour burst detected (PAL or SECAM)
CODE	colour information 0 = no colour detected 1 = colour detected
X	for future enhancements, do not evaluate

Note

1. Software model of SAA7196 compatible with ID3 to ID0 = 0; version V0 (first version).

8.3 Decoder part

Table 16 I²C-bus decoder control; subaddress and data bytes for writing (X in address byte = 0; 40H at I²CSA = LOW or 42H at I²CSA = HIGH)

FUNCTION SUBADDRESS		DATA								DF(1)
		D7	D6	D5	D4	D3	D2	D1	D0	
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	
H-sync begin; 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0	
H-sync stop; 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0	
H-clamp begin; 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0	
H-clamp stop; 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0	
H-sync after PHI1; 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0	
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0	
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0	
Colour-killer QUAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0	
Colour-killer SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0	
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0	
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0	
Chroma gain control	0C	COLO	LFIS1	LFIS0	0	0	0	0	0	
Standard/mode control	0D	VTRC	0	0	0	RTSE	HRMV	SSTB	SECS	
I/O and clock control	0E	HPLL	0	OECL	OEHV	OEYC	CHRS	GPSW2	GPSW1	
Control #1	0F	AUFD	FSEL	SXCR	SCEN	0	YDEL2	YDEL1	YDEL0	
Control #2	10	0	0	0	0	0	HRFS	VNOI1	VNOI0	
Chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0	
Chroma saturation	12	0	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0	
Luminance contrast	13	0	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0	
H-sync begin; 60 Hz	14	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	
H-sync stop; 60 Hz	15	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	HS6B7	
H-clamp begin; 60 Hz	16	HC6B7	HC6B7	HC6B7	HC6B7	HC6B7	HC6B7	HC6B7	HC6B7	
H-clamp stop; 60 Hz	17	HC6S7	HC6S7	HC6S7	HC6S7	HC6S7	HC6S7	HC6S7	HC6S7	
H-sync after PHI1: 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0	
Luminance brightness	19	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
Reserved	1A to 1F	0	0	0	0	0	0	0	0	

Note

1. Default register contents to be filled in by hand.

Table 17 Function of the register bits of Table 16 for subaddresses ‘00’ to ‘19’

SUBADDRESS	DESCRIPTION
IDEL7 to IDEL0 ‘00’	Increment delay time (dependent on application), step size = 4/LLC. The delay time is selectable from –4/LLC (–1 decimal multiplier) to –1024/LLC (–256 decimal multiplier) equals data FFH to 00H. A sign-bit, designated A08 and internally set HIGH, indicates always negative values. The maximum delay time in 60 Hz systems is –780 equally to 3DH; the maximum delay time in 50 Hz systems is –944 equally to 14H. Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown (the horizontal PLL does not operate if the maximum delays are exceeded; the system clock frequency is set to a value of the last update and is within ±7.1% of nominal frequency).
HSYB7 to HSYB0 ‘01’	Horizontal sync begin for 50 Hz, step size = 2/LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) and equals data BFH to C0H. Two’s complement numbers with ‘hidden’ sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB-1 bits.
HSYS7 to HSYS0 ‘02’	Horizontal sync stop for 50 Hz, step size = 2/LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BFH to C0H. Two’s complement numbers with ‘hidden’ sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB-1 bits.
HCLB7 to HCLB0 ‘03’	Horizontal clamp start for 50 Hz, step size = 2/LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7FH to 80H.
HCLS7 to HCLS0 ‘04’	Horizontal clamp stop for 50 Hz, step size = 2/LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7FH to 80H.
HPHI7 to HPHI0 ‘05’	Horizontal sync start after PHI1 for 50 Hz, step size = 8/LLC. The delay time is selectable from –32 to +31.7 μs (+118 to –118 decimal multiplier) equals data 75H to 8AH . Forbidden, outside available central counter range, are +127 to +118 decimal multiplier equals data 7EH to 76H as well as –119 to –128 decimal multiplier equals data 89H to 80H.
BYPS ‘06’	input mode select bit 0 = CVBS mode (chrominance trap active) 1 = S-Video mode (chrominance trap bypassed)
PREF ‘06’	use of prefilter 0 = prefilter off (bypassed) 1 = prefilter on; PREF may be used if chrominance trap is active
BPSS1 to BPSS0 ‘06’	Aperture band-pass to select different characteristics with maximums (0.2 to 0.3 × LLC/2); see Table 18 and Figs 19 to 28.
CORI1 to CORI0 ‘06’	Coring range for high frequency components according to 8-bit luminance; see Table 19 and Fig.18.
APER1 and APER0 ‘06’	Aperture band-pass filter weights high frequency components of luminance signal; see Table 20 and Figs 19 to 28.
HUE7 to HUE0 ‘07’	Hue control from +178.6° to –180.0° equals data bytes 7FH to 80H; 0° equals 00.

SUBADDRESS	DESCRIPTION
CKTQ4 to CKTQ0 ‘08’	Colour-killer threshold QAM (PAL, NTSC) from approximately −30 dB to −18 dB equals data bytes F8H to 07H.
CKTS4 to CKTS0 ‘09’	Colour-killer threshold SECAM from approximately −30 dB to −18 dB equals data bytes F8H to 07H.
PLSE7 to PLSE0 ‘0A’	PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction) equals FFH to 00H, MEDIUM equals 80.
SESE7 to SESE0 ‘0B’	SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction) equals FFH to 00H, MEDIUM equals 80.
COLO ‘0C’	colour-on bit 0 = automatic colour-killer 1 = forced colour-on
LFIS1 to LFIS0 ‘0C’	Automatic gain control (AGC filter); see Table 21.
VTRC ‘0D’	VTR/TV mode bit 0 = TV mode 1 = VTR mode
RTSE ‘0D’	real time output mode select bit 0 = PLIN switched to output RTS1 (pin 34); ODD switched to RTS0 (pin 35) 1 = HL switched to output RTS1 (pin 34); VL switched to RTS0 (pin 35)
HRMV ‘0D’	HREF position select 0 = default 1 = HREF is 8 × LLC2 clocks earlier
SSTB	status byte select 0 = status byte 0 is selected 1 = status byte 1 is selected
SECS ‘0D’	SECAM mode bit 0 = other standards 1 = SECAM
HPLL ‘0E’	horizontal clock PLL 0 = PLL closed 1 = PLL open and horizontal frequency fixed
OECL ‘0E’	select internal/external clock source 0 = LLCB and CREFB are inputs 1 = LLCB and CREFB are outputs
OEHV ‘0E’	output enable of horizontal/vertical sync 0 = HS, HREF and VS pins are inputs (outputs high-impedance) 1 = HS, HREF and VS pins are outputs
OEYC ‘0E’	data output YUV15 to YUV0 enable 0 = data pins are inputs 1 = data pins are controlled by DIR (pin 95)

SUBADDRESS	DESCRIPTION
CHRS '0E'	S-VHS bit (chrominance from CVBS or from chrominance input) 0 = controlled by bit BYPS (subaddress 06) 1 = chrominance from chrominance input CHR7 to CHR0
GPSW2 and GPSW1 '0E'	general purpose switches; see Table 22
AUFD '0F'	automatic field detection 0 = field selection by bit FSEL 1 = automatic field detection by SAA7196
FSEL '0F'	field select (bit AUFD = 0) 0 = 50 Hz (625 lines) 1 = 60 Hz (525 lines)
SXCR '0F'	SECAM cross-colour reduction 0 = reduction off 1 = reduction on
SCEN '0F'	enable sync and clamping pulse 0 = HSY and HCL outputs HIGH (pins 25 and 26) 1 = HSY and HCL outputs active
YDEL2 to YDEL0 '0F'	luminance delay compensation; see Table 23
HRFS '10'	select HREF position 0 = normal, HREF is matched to YUV output on expansion port 1 = HREF is matched to CVBS input port
VNOI1 to VNOI0 '10'	vertical noise reduction; see Table 24
CHCV7 to CHCV0 '11'	chrominance gain control (nominal values) for QAM-modulated input signals, effects UV output amplitude (SECAM with fixed gain); see Table 25
SATN6 to SATN0 '12'	chrominance saturation control for VRAM port; see Table 26
CONT6 to CONT0 '13'	luminance contrast control for VRAM port; see Table 27
HS6B7 to HS6B0 '14'	Horizontal sync begin for 60 Hz, step size = 2/LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BFH to C0H. Two's complement numbers with 'hidden' sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB-1 bits.
HS6S7 to HS6S0 '15'	Horizontal sync stop for 60 Hz, step size = 2/LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BFH to C0H. Two's complement numbers with 'hidden' sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB-1 bits.
HC6B7 to HC6B0 '16'	Horizontal clamp begin for 60 Hz, step size = 2/LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) and equals data 7FH to 80H.

SUBADDRESS	DESCRIPTION
HC6S7 to HC6S0 '17'	Horizontal clamp stop for 60 Hz, step size = 2/LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7FH to 80H.
HP6I7 to HP6I0 '18'	Horizontal sync start after PHI1 for 60 Hz, step size = 8/LLC. The delay time is selectable from –32 to +31.7 µs (+97 to –97 decimal multiplier) equals data 61H to 9FH. Forbidden, outside available central counter range, are +127 to +98 decimal multiplier equals data 7EH to 62H as well as –98 to –128 decimal multiplier equals data 9EH to 80H.
BRIG7 to BRIG0 '19'	luminance brightness control for VRAM port; see Table 28

Table 18 Aperture band-pass to select different characteristics with maximums (0.2 to 0.3 × ½LLC); for characteristics see Figs 19 to 28

BIT	
BPSS1	**BPSS0**
0	0
0	1
1	0
1	1

Table 19 Coring range for high frequency components according to 8-bit luminance

BIT		CORING
CORI1	**CORI0**	
0	0	coring off
0	1	±1 LSB of 8-bit
1	0	±2 LSB of 8-bit
1	1	±3 LSB of 8-bit

Table 20 Aperture band-pass filter weights high frequency components of luminance signal; for characteristics see Figs 19 to 28

BIT		FACTOR
APER1	**APER0**	
0	0	0
0	1	0.25
1	0	0.5
1	1	1

Table 21 Automatic gain control (AGC filter)

BIT		LOOP FILTER TIME CONSTANT
LFIS1	**LFIS0**	
0	0	slow
0	1	medium
1	0	fast
1	1	actual gain stored (for test purposes only)

Table 22 General purpose switches

BIT		SET PORT OUTPUT PINS
GPSW2 (PIN 32)	**GPSW1 (PIN 33)**	
0	0	use is dependent on application
0	1	
1	0	
1	1	

Table 23 Luminance delay compensation

BIT			DELAY[1]
YDEL2	**YDEL1**	**YDEL0**	
0	0	0	$0 \times 2/LCC$
0	0	1	$+1 \times 2/LCC$
0	1	0	$+2 \times 2/LCC$
0	1	1	$+3 \times 2/LCC$
1	0	0	$-4 \times 2/LCC$
1	0	1	$-3 \times 2/LCC$
1	1	0	$-2 \times 2/LCC$
1	1	1	$-1 \times 2/LCC$

Note

1. Step size = 2/LCC = 67.8 ns for 50 Hz and 81.5 ns for 60 Hz.

Table 24 Vertical noise reduction

BIT		MODE
VNOI1	**VNOI0**	
0	0	normal
0	1	searching window
1	0	free-running mode
1	1	vertical noise reduction bypassed

Table 25 Chrominance gain control; note 1

BIT								GAIN
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
1	1	1	1	1	1	1	1	maximum gain
.	.	.	.	.	.	.	.	to
0	1	0	1	1	0	0	1	CCIR level for PAL
.	.	.	.	.	.	.	.	to
0	0	1	0	1	1	0	0	CCIR level for NTSC
.	.	.	.	.	.	.	.	to
0	0	0	0	0	0	0	0	minimum gain

Note

1. Default programmed values dependent on application.

Table 26 Chrominance saturation control for VRAM port

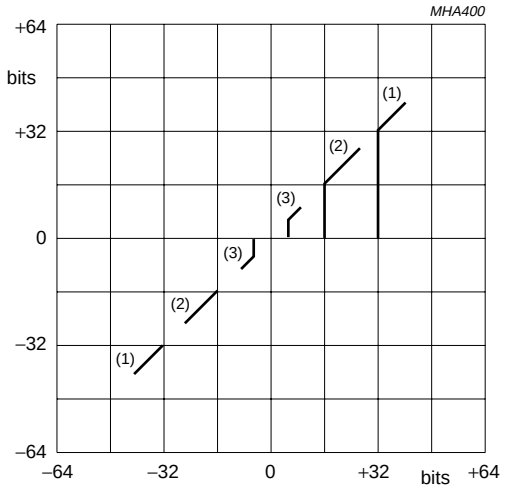
BIT								GAIN
D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	1	1	1	1	1	1.999 (maximum saturation)
.	.	.	.	.	.	.	.	to
0	1	0	0	0	0	0	0	1 (CCIR level)
.	.	.	.	.	.	.	.	to
0	0	0	0	0	0	0	0	0 (colour off)

Table 27 Luminance contrast control for VRAM port

BIT								GAIN
D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	1	1	1	1	1	1.999 (maximum contrast)
.	.	.	.	.	.	.	.	to
0	1	0	0	0	0	0	0	1 (CCIR level)
.	.	.	.	.	.	.	.	to
0	0	0	0	0	0	0	0	0 (luminance off)

Table 28 Luminance brightness control for VRAM port

BIT								GAIN
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	255 (bright)
.	.	.	.	.	.	.	.	to
1	0	0	0	0	0	0	0	128 (CCIR level)
.	.	.	.	.	.	.	.	to
0	0	0	0	0	0	0	0	0 (dark)



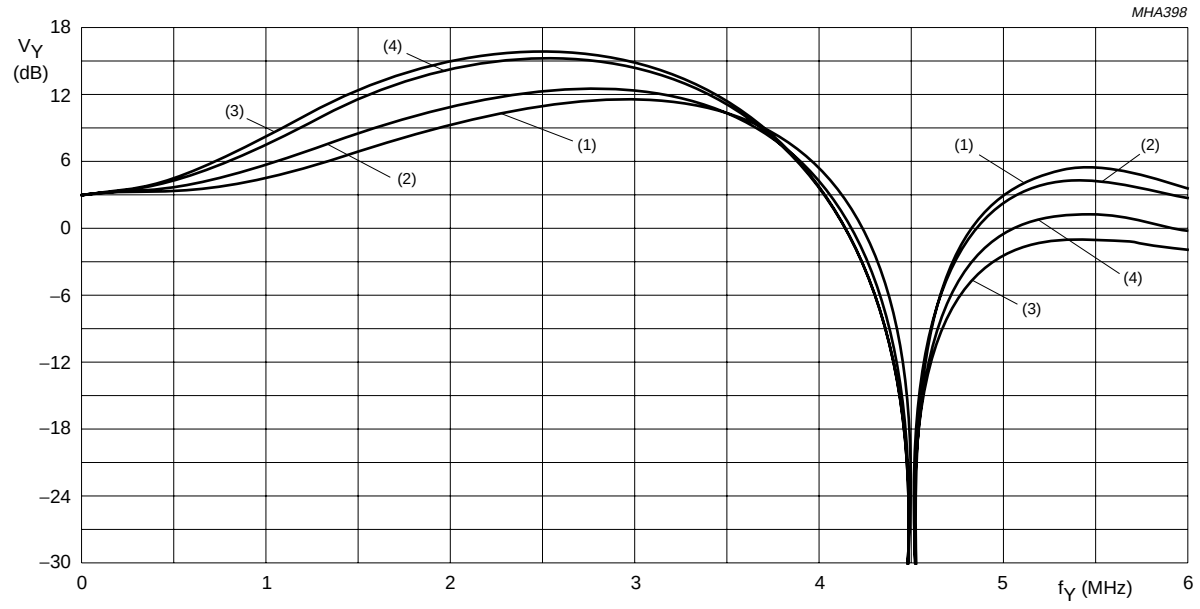
The tresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output).

(1) CORI1 = 1; CORI0 = 1

(2) CORI1 = 1; CORI0 = 0

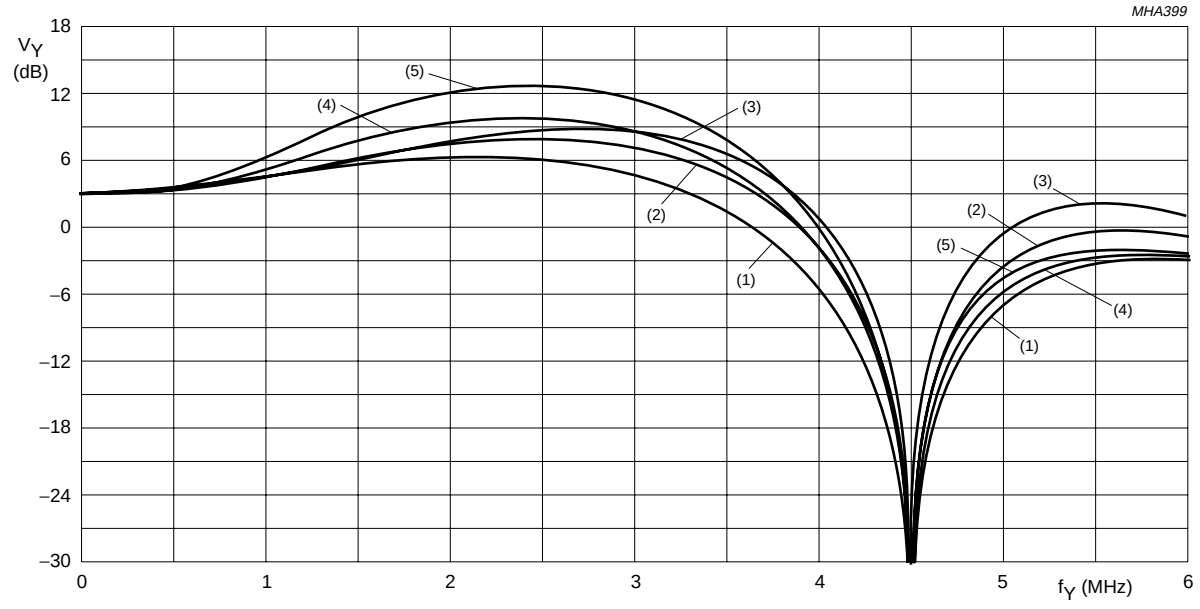
(3) CORI1 = 0; CORI0 = 1

Fig.18 Coring function adjustment by subaddress 06 to affect the band filter output signal.



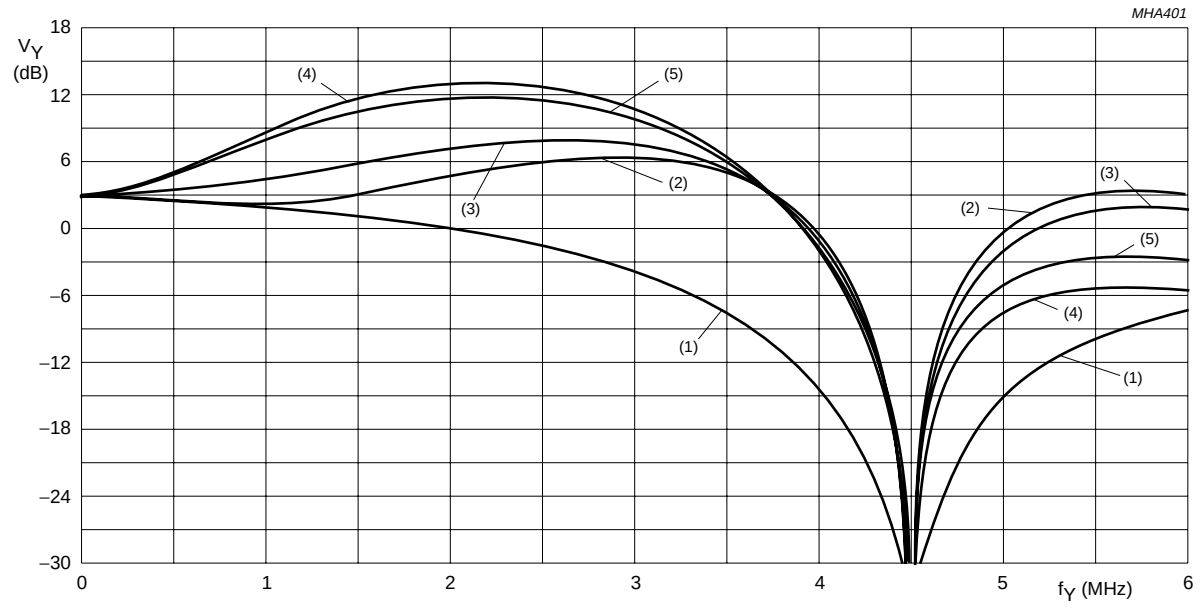
(1) 43H. (2) 53H. (3) 63H. (4) 73H.

Fig.19 Luminance control in 50 Hz/CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture band-pass filter characteristic.



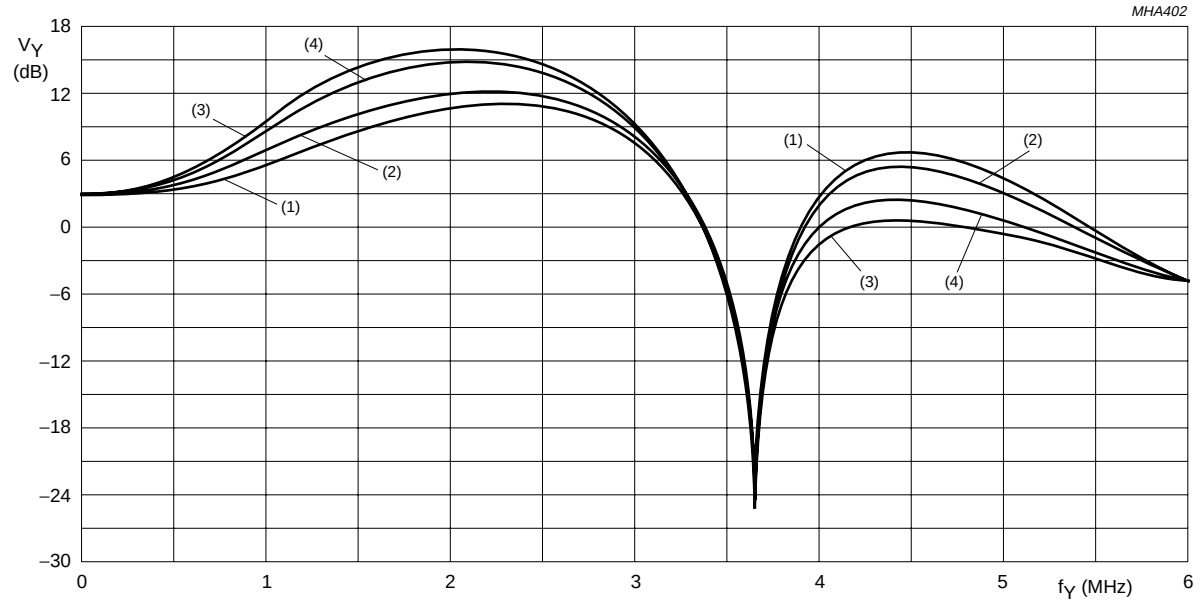
(1) 40H. (2) 41H. (3) 42H. (4) 61H. (5) 62H.

Fig.20 Luminance control in 50 Hz/CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture band-pass filter characteristic.



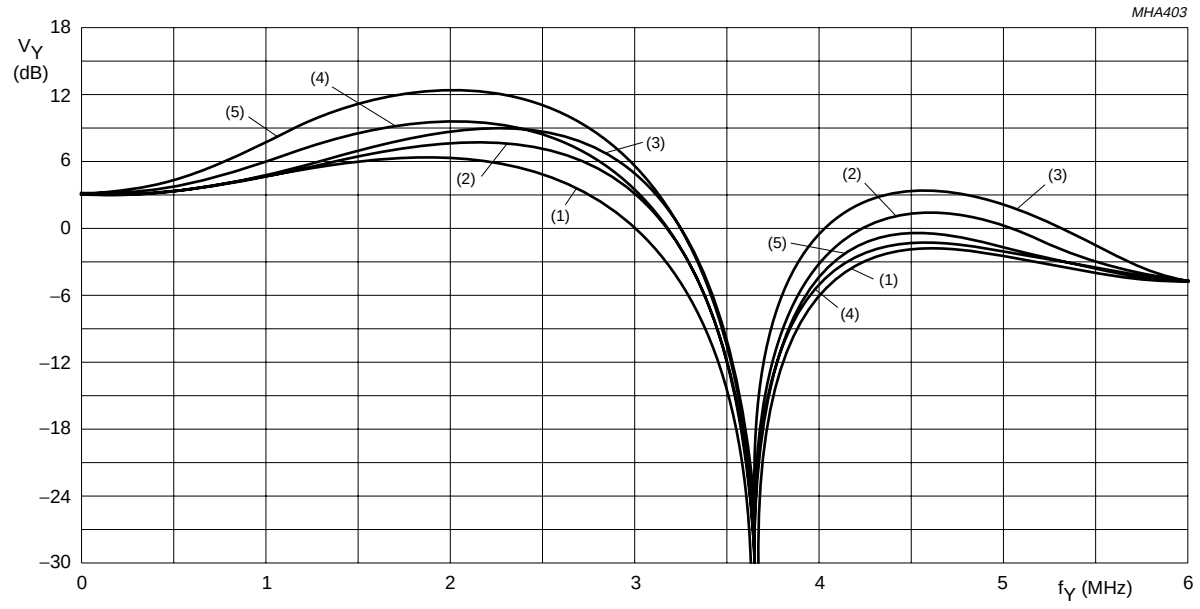
(1) 00H. (2) 03H. (3) 13H. (4) 23H. (5) 33H.

Fig.21 Luminance control in 50 Hz/CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture band-pass filter characteristic.



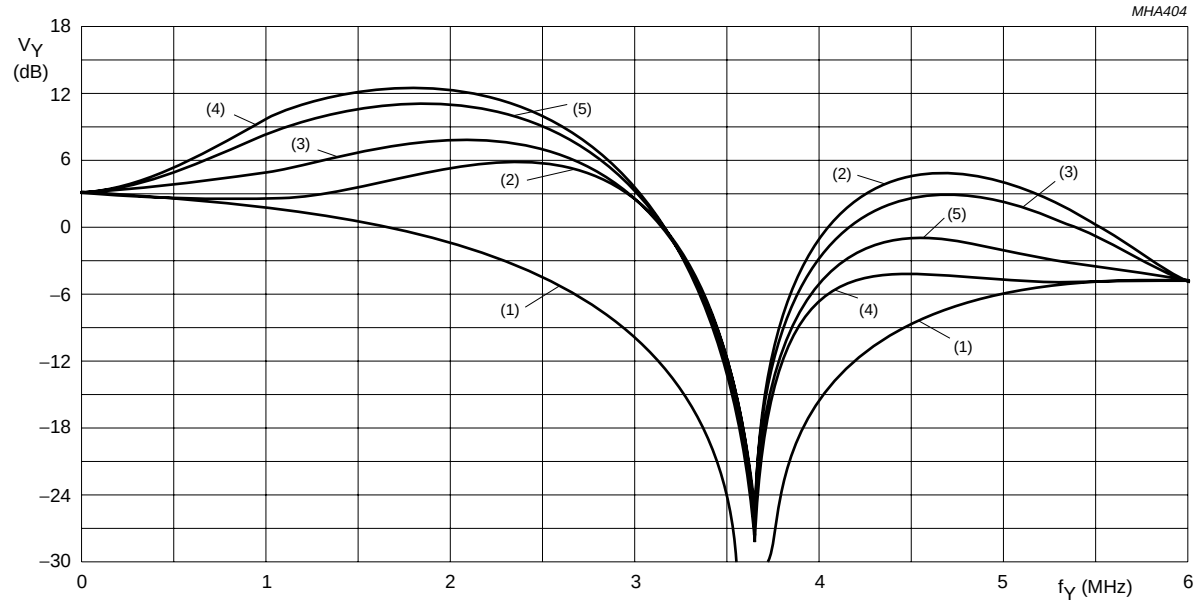
(1) 43H. (2) 53H. (3) 63H. (4) 73H.

Fig.22 Luminance control in 60 Hz/CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture band-pass filter characteristics.



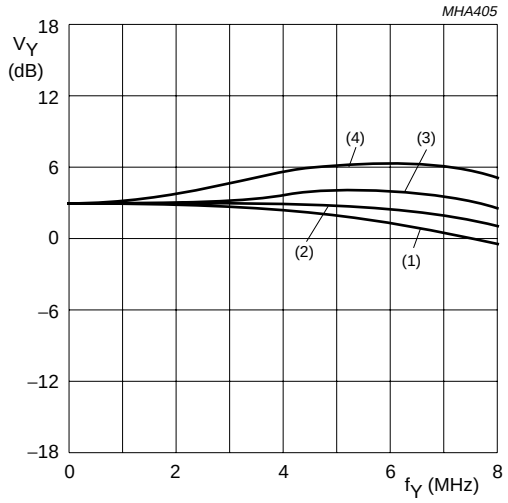
(1) 40H. (2) 41H. (3) 42H. (4) 61H. (5) 62H.

Fig.23 Luminance control in 60 Hz/CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture band-pass filter characteristics.



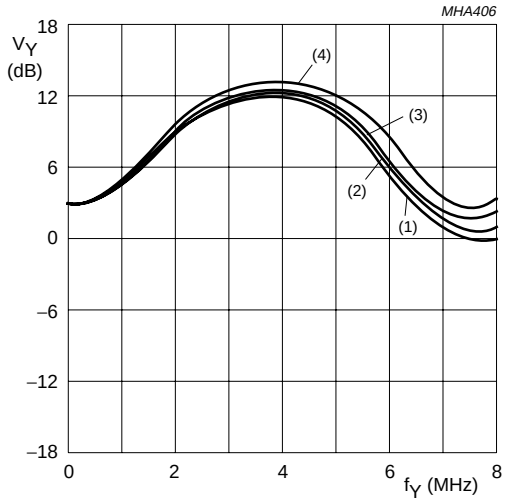
(1) 00H. (2) 03H. (3) 13H. (4) 23H. (5) 33H.

Fig.24 Luminance control in 60 Hz/CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture band-pass filter characteristics.



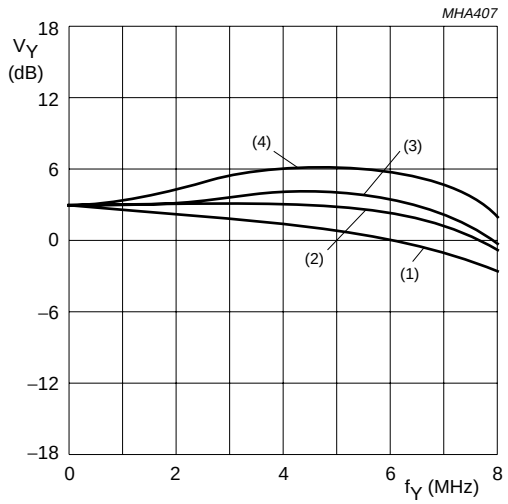
(1) 80H. (2) 81H. (3) 82H. (4) 83H.

Fig.25 Luminance control in 50 Hz/S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture band-pass filter characteristics.



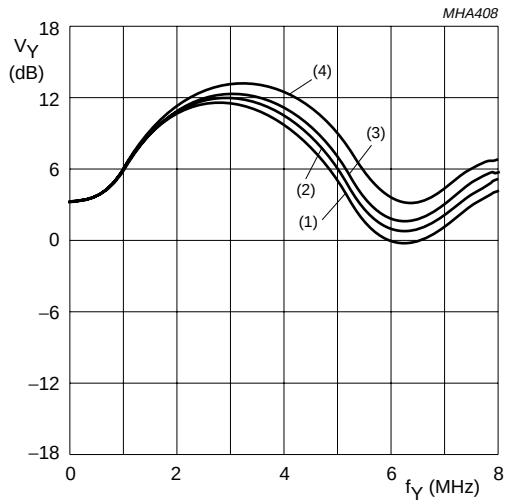
(1) C0H. (2) C1H. (3) C2H. (4) C3H.

Fig.26 Luminance control in 50 Hz/S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture band-pass filter characteristics.



(1) 80H. (2) 81H. (3) 82H. (4) 83H.

Fig.27 Luminance control in 60 Hz/S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture band-pass filter characteristics.



(1) C0H. (2) C1H. (3) C2H. (4) C3H.

Fig.28 Luminance control in 60 Hz/S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture band-pass filter characteristics.

8.4 Scaler part

Table 29 I²C-bus scaler control; subaddress and data bytes for writing

FUNCTION SUBADDRESS		DATA								DF(1)
		D7	D6	D5	D4	D3	D2	D1	D0	
Formats and sequence	20	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	
Output data pixel/line(2)	21	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
Input data pixel/line(2)	22	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
Horizontal window start(2)	23	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Horizontal filter	24	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field(3)	25	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
Input data lines/field(3)	26	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
Vertical window start(3)	27	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical Y processing	28	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start(4)	29	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
Vertical bypass count(4)	2A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
	2B	0	0	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	2C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	2D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	2E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	2F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Data path setting(5)	30	VOF	AFG	LLV	MCT	QPL	QPP	TTR	EFE	
Unused	31 to 3F									

Notes

1. Default register contents to be filled in by hand.
2. Continued in ‘24’.
3. Continued in ‘28’.
4. Continued in ‘2B’.
5. Data representation, transfer mode and adaptivity.

Table 30 Function of the register bits of Table 29 for subaddresses ‘20’ to ‘30’

SUBADDRESS	DESCRIPTION
RTB ‘20’	ROM table bypass switch 0 = anti-gamma ROM active 1 = table is bypassed
OF1 to OF0	set output field mode; see Table 31
VPE	VRAM port outputs enable 0 = HFL and INCADR inactive (HFL = LOW, INCADR = HIGH); VRO outputs in 3-state 1 = HFL and INCADR enabled; VRO outputs dependent on $\overline{VOE}$
LW1 to LW0 ‘20’	first pixel position in VRO data FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1 (YUV); see Table 32 FS1 = 1; FS0 = 1 (monochrome); see Table 33
FS1 to FS0	FIFO output register format select (bit EFE see ‘30’); see Table 34
XD9 to XD0 ‘21 and 24’	pixel number per line (straight binary) on output (VRO): 00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum; take care of vertical processing)
XS9 to XS0 ‘22 and 24’	pixel number per line (straight binary) on inputs (YIN and UVIN): 00 0000 0000 to 11 1111 1111 (number of input pixels per line as a maximum; take care of vertical processing)
XO8 to XO0 ‘23 and 24’	Horizontal start position (straight binary) of scaling window (take care of active pixel number per line): start with the 1st pixel after HREF rise = 0 0000 0011 to 1 1111 1111 (003 to 1FF). Window start and window end may be cut by internal delay compensated HREF = 0 phase.
HF2 to HF0 ‘24’	Horizontal decimation filter; the filter coefficients are related to the luminance path. The filter coefficient may differ from upper table when a combination with vertical Y processing and adaptive modes are provided. See Table 35.
YD9 to YD0 ‘25 and 28’	line number per output field (straight binary): 00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)
YS9 to YS0 ‘26 and 28’	line number per input field (straight binary) 00 0000 0000 for 0 line 11 1111 1111 for 1023 lines (maximum = number of lines/field – 3)
YO8 to YO0 ‘27 and 28’	Vertical start of scaling window [take care of active line number per field (straight binary); window start and window end may be cut by the external VS signal] 0 0000 0000; start with 3rd line after the rising slope of VS 0 0000 0011; start with 1st line after the falling slope of nominal VS (7151B, 7191B input) 1 1111 1111; 511 + 3 lines after the rising slope of VS (maximum value)
AFS ‘28’	adaptive filter switch 0 = off; use VP1, VP0 and HF2 to HF0 bits 1 = on; filter characteristics are selected by the scaler
VP1 to VP0	vertical luminance data processing; see Table 36
VS8 to VS0 ‘29 and 2B’	vertical bypass start, sets begin of the bypass region (straight binary); scaling region overrides bypass region (YO bits) 0 0000 0000; start with 3rd line after the rising slope of VS 0 0000 0011; start with 1st line after the falling slope of nominal VS (7151B, 7191B input) 1 1111 1111; 511 + 3 lines after the rising slope of VS (maximum value)

VC8 to VC0 ‘29 and 2B’	vertical bypass count, sets length of bypass region (straight binary) 0 0000 0000; 0 line length 1 1111 1111; 511 lines length (maximum = number of lines/field – 3)
POE	polarity, internally detected odd/even flag O/E 0 = flag unchanged 1 = flag inverted
VL7 to VL0 ‘2C’	set lower limit V for colour-keying (8-bit; two’s complement) 1000 0000; as maximum negative value = –128 signal level 0000 0000; limit = 0 0111 1111; as maximum positive value = +127 signal level
VU7 to VU0 ‘2D’	set upper limit V for colour-keying (8-bit; two’s complement) 1000 0000; as maximum negative value = –128 signal level 0000 0000; limit = 0 0111 1111; as maximum positive value = +127 signal level
UL7 to UL0 ‘2E’	set lower limit V for colour-keying (8-bit; two’s complement) 1000 0000; as maximum negative value = –128 signal level 0000 0000; limit = 0 0111 1111; as maximum positive value = +127 signal level
UU7 to UU0 ‘2F’	set upper limit V for colour-keying (8-bit; two’s complement) 1000 0000; as maximum negative value = –128 signal level 0000 0000; limit = 0 0111 1111; as maximum positive value = +127 signal level
VOF ‘30’	VRAM bus output format 0 = enabling of 32 to 16-bit multiplexing via VMUX (pin 46) 1 = disabling of 32 to 16-bit multiplexing via VMUX (pin 46)
AFG	adoptive geometrical filter 0 = linear H and V data processing 1 = approximated geometrical H and V interpolation (improved scaling accuracy of luminance)
LLV	luminance limiting value 0 = amplitude range between 1 and 254 1 = amplitude range between 16 and 235, suitable for monochrome and YUV modes
MCT	monochrome and two’s complement output data select 0 = inverse gray scale luminance (if gray scale is selected by FIS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if gray scale is selected by FS bits) or two’s complement U, V data output
QPL	line qualifier polarity flag 0 = LNQ is active-LOW (pin 52) 1 = LNQ is active-HIGH

QPP	pixel qualifier polarity flag 0 = PXQ is active-LOW (pin 51) 1 = PXQ is active-HIGH
TTR	transparent data transfer 0 = normal operation (VRAM data burst transfer) 1 = FIFO register transparent
EFE	extended formats enable bit (see FS bits in subaddress ‘20’) 0 = 32-bit long word output formats 1 = extended output formats (‘one pixel a time’)

Table 31 Set output field mode

BIT		MODE
OF1	**OF0**	
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only (odd fields ignored) for non-interlaced storage

Table 32 First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1 (YUV)

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	CONDITIONS
0	0	pixel 0	pixel 0	pixel 1	pixel 1	EFE = 0; TTR = 0
0	1	pixel 0	pixel 0	pixel 1	pixel 1	
1	0	black	black	pixel 0	pixel 0	
1	1	black	black	pixel 0	pixel 0	

Table 33 First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome); note 1

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	CONDITIONS
0	0	pixel 0	pixel 1	pixel 2	pixel 3	EFE = 0; TTR = 0
0	1	black	pixel 0	pixel 1	pixel 2	
1	0	black	black	pixel 0	pixel 1	
1	1	black	black	black	pixel 0	
0	0	pixel 0	pixel 1	X	X	EFE = 1; TTR = 0; LW only effects the gray scale format
0	1	black	pixel 0	X	X	
1	0	pixel 0	pixel 1	X	X	
1	1	black	pixel 0	X	X	

Note

1. X = don’t care.

Table 34 FIFO output register format select (bit EFE; see '30')

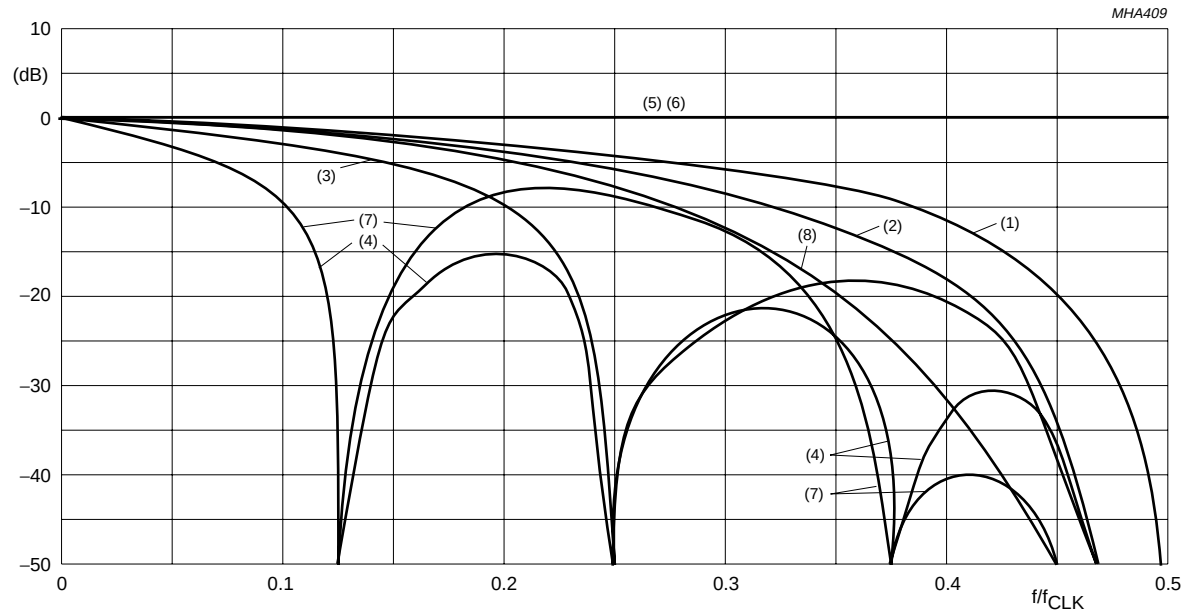
EFE	FS1	FS0	**OUTPUT FORMAT** (Tables 8 to 11)
0	0	0	RGB 5-5-5+α; 2 × 16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4 : 2 : 2; 2 × 16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4 : 2 : 2; 1 × 16-bit/pixel; 16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4 × 8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB 5-5-5+α; 1 × 16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4 : 2 : 2+α; 1 × 16-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format
1	1	0	RGB 8-8-8+α; 1 × 24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2 × 8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

Table 35 Horizontal decimation filter

HF2	HF1	HF0	TAPS	**FILTER** (see Figs 29 and 30)
0	0	0	2	filter 1
0	0	1	3	filter 2
0	1	0	5	filter 3
0	1	1	9	filter 4
1	0	0	1	filter bypassed
1	0	1	1	filter bypassed + delay in Y channel of 1T
1	1	0	8	filter 5
1	1	1	4	filter 6

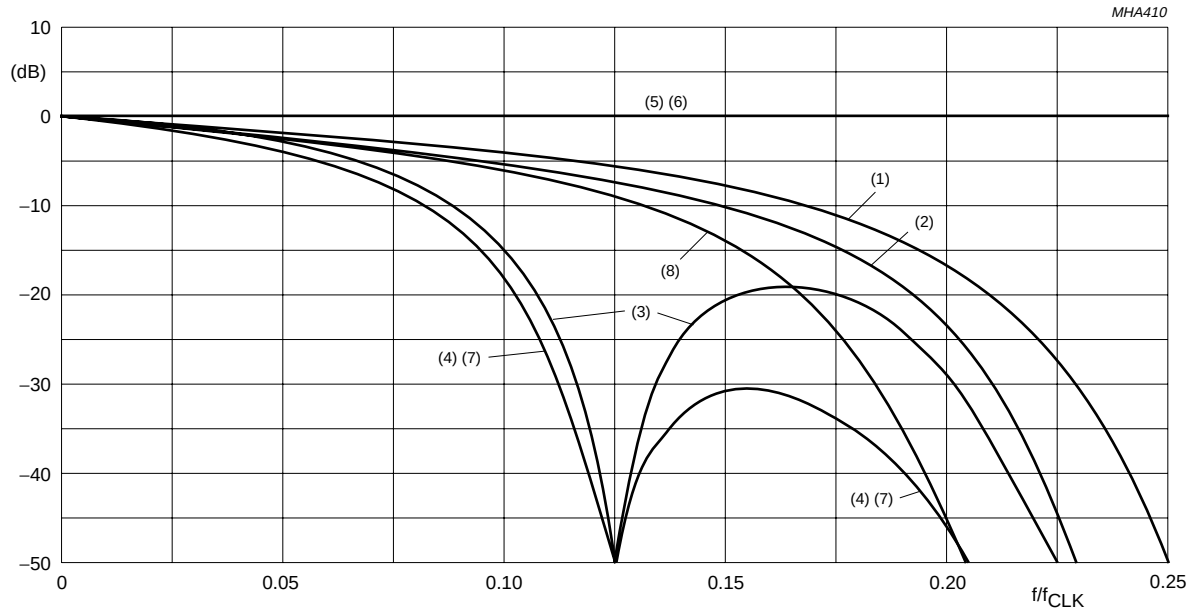
Table 36 Vertical luminance data processing

VP1	VP0	**PROCESSING (APPROXIMATE EQUATIONS)**
0	0	bypassed
0	1	delay of one line $H(z) = z^{-H}$
1	0	vertical filter 1: $[H(z) = \frac{1}{2}(1 + z^{-H})]$
1	1	vertical filter 2: $[H(z) = \frac{1}{4}(1 + 2z^{-H} + z^{-2H})]$



(1) 000. (2) 001. (3) 010. (4) 011. (5) 100. (6) 101. (7) 110. (8) 111.

Fig.29 Horizontal frequency characteristic of luminance signal (Y) dependent on HF2 to HF0 bits (subaddress 24).



(1) 000. (2) 001. (3) 010. (4) 011. (5) 100. (6) 101. (7) 110. (8) 111.

Fig.30 Horizontal frequency characteristic of chrominance signals (UV) without UV interpolation dependent on HF2 to HF0 bits (subaddresses 24).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pins 14, 27, 31, 45, 61, 77, 91 and 106		–0.5	+6.5	V
V_I	voltage on all input/output pins		–0.5	V_{DD} + 0.5	V
V_{es}	electrostatic handling for all pins	note 1	–	±2000	V
P_{tot}	total power dissipation		–	1.5	W
T_{stg}	storage temperature range		–65	+150	°C
T_{amb}	operating ambient temperature range		0	70	°C

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10 CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage; pins 14, 31, 45, 61, 77, 91 and 106		4.5	5	5.5	V
V_{DDA}	analog supply voltage; pin 27		4.5	5	5.5	V
I_{DDD}	digital supply current	inputs LOW; outputs without load	–	170	260	mA
I_{DDA}	analog supply current		–	10	20	mA
Data, clock and control inputs						
V_{IL}	LOW level input voltage	clocks	–0.5	–	+0.6	V
		other inputs	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	clocks	2.4	–	V_{DD} + 0.5	V
		other inputs	2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_{IL} = 0	–	–	10	µA
C_I	input capacitance data		–	–	8	pF
	input capacitance clocks		–	–	10	pF
	input capacitance 3-state I/O	high-impedance state	–	–	8	pF
Data and control outputs; note 1						
V_{OL}	LOW level output voltage		0	–	0.6	V
V_{OH}	HIGH level output voltage		2.4	–	V_{DD}	V
LFCO output (pin 28)						
$V_{o(p-p)}$	LFCO output signal (peak-to-peak value)		1.4	2.1	2.6	V
V_{28}	output voltage		1	–	V_{DD}	V

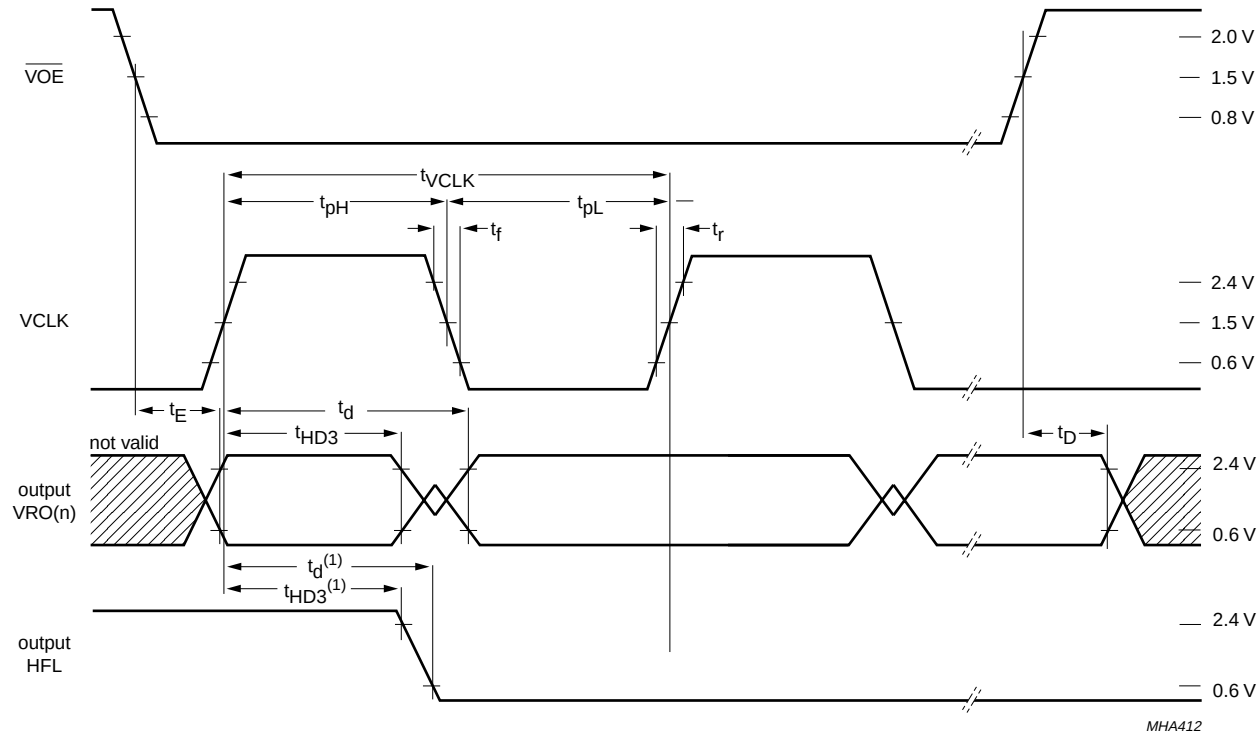
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus, SDA and SCL (pins 3 and 4)						
V_{IL}	LOW level input voltage		–0.5	–	+1.5	V
V_{IH}	HIGH level input voltage		3	–	V_{DD} + 0.5	V
$I_{3,4}$	input current		–	–	±10	µA
I_{ACK}	output current on pin 3	acknowledge	3	–	–	mA
V_{OL}	output voltage at acknowledge	I_3 = 3 mA	–	–	0.4	V
Clock input timing (LLCB); see Fig.32						
T_{cy}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCBH}/t_{LLCB}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
Data, control and CREFB input timing; see Figs 32 and 33 and note 2						
t_{SU}	set-up time		11	–	–	ns
t_{HD1}	hold time		4	–	–	ns
Data and control output timing; see Fig.32 and note 3						
C_L	load capacitance	data, HREF and VS	15	–	50	pF
		control	7.5	–	25	pF
t_{HD2}	output hold time	C_L = 15 pF	13	–	–	ns
t_{PD}	propagation delay from negative edge of LLCB	data, HREF and VS; C_L = 50 pF	–	–	29	ns
		control; C_L = 25 pF	–	–	29	ns
t_{PZ}	propagation delay from negative edge of LLCB (to 3-state)	note 4	–	–	15	ns
Clock output timing (LLC, LLC2 and LLCB); see Fig.32						
C_L	output load capacitance		15	–	40	pF
t_{LLC},t_{LLCB}	cycle time		31	–	45	ns
t_{LLC2}	cycle time		62	–	90	ns
δ	duty factor	t_{LLCH}/t_{LLC} t_{LLC2H}/t_{LLC2} t_{LLCBH}/t_{LLCB}	40	50	60	%
t_r	rise time	0.6 to 2.6 V	–	–	5	ns
t_f	fall time	2.6 to 0.6 V	–	–	5	ns
t_{dLLC2}	delay between $LLCB_{out}$ and $LLC2_{out}$	at 1.5 V, 40 pF	–	–	8	ns
Data qualifier output timing (CREFB); see Fig.32						
t_{HD3}	output hold time	C_L = 15 pF	3	–	–	ns
t_{PD}	propagation delay from positive edge of LLCB	C_L = 40 pF	–	–	18	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz system	–	15625	–	Hz
		60 Hz system	–	15734	–	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation	50 Hz system	–	–	±5.6	%
		60 Hz system	–	–	±6.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL	–	4.433618	–	MHz
		NTSC	–	3.579545	–	MHz
Δf_{SC}	lock-in range	PAL/NTSC	±400	–	–	Hz
Crystal oscillator; see Fig.34 and note 5						
f_n	nominal frequency	3rd harmonic	–	26.8	–	MHz
$\Delta f/f_n$	permissible deviation f_n		–	–	±50	ppm
	temperature deviation from f_n		–	–	±20	ppm
CRYSTAL SPECIFICATION; note 6						
T_{amb}	temperature range		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_S	series resonance resistance		–	50	80	Ω
C_1	motional capacitance		–	1.1 ±20%	–	pF
C_0	parallel capacitance		–	3.5 ±20%	–	pF
VCLK timing; see Fig.31 and note 7						
t_{VCLK}	VRAM port clock cycle time	note 8	50	–	200	ns
t_{pL}, t_{pH}	LOW and HIGH times	note 9	17	–	–	ns
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
VRO and reference signal output timing; see Fig.31						
C_L	output load capacitance	VRO outputs	15	–	40	pF
		other outputs	7.5	–	25	pF
$t_{HD;DAT}$	VRO data hold time	C_L = 10 pF; note 10	0	–	–	ns
		related to LCCB (INCADR, HFL); C_L = 10 pF; note 11	0	–	–	ns
		related to VCLK (HFL); C_L = 10 pF; note 11	0	–	–	ns
t_d	VRO data delay time	C_L = 40 pF; note 10	–	–	25	ns
		related to LCCB (INCADR, HFL); C_L = 25 pF; note 11	–	–	60	ns
		related to VCLK (HFL); C_L = 25 pF; note 11	–	–	60	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_D	VRO disable time to 3-state	C_L = 40 pF; note 12	–	–	40	ns
		C_L = 25 pF; note 13	–	–	24	ns
t_E	VRO enable time from 3-state	C_L = 40 pF; note 12	–	–	40	ns
		C_L = 25 pF; note 13	–	–	25	ns
Response times to HFL flag						
$t_{HFL\ VOE}$	HFL rising edge to VRAM port enable		–	–	810	ns
$t_{HFL\ VCLK}$	HFL rising edge to VCLK burst		–	–	840	ns

Notes

1. Levels measured with load circuits dependent on output type. Control outputs (HREF and VS excluded): 1.2 kΩ at 3 V (TTL load) and C_L = 25 pF. Data, HREF and VS outputs: 1.2 kΩ at 3 V (TTL load) and C_L = 50 pF.
2. Data input signals are CVBS7 to CVBS0, CHR7 to CHR0 (related to LLC) and YUV15 to YUV0. Control input signals are HREF, VS and DIR.
3. Data outputs are YUV15 to YUV0. Control outputs are HREF, VS, HS, HSY, HCL, SODD, SVS, SHREF, PXQ, LNQ, RTCO, RTS1 and RTS0.
4. The minimum propagation delay from 3-state to data active is 0 related to the falling edge of LLCB.
5. If the internal oscillator is not being used, the applied clock signal must be TTL-compatible.
6. Philips catalogue number 9922 520 30004.
7. CREFB-timing also valid for VCLK in transparent mode (see Fig.32).
8. Maximum t_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
9. Measured at 1.5 V level; t_{pL} may be infinite.
10. Timings of VRO refer to the rising edge of VCLK.
11. The timing of INCADR refers to LLCB; the rising edge of HFL always refers to LLCB. During a VRAM transfer, the falling edge of HFL is generated by VCLK. Both edges of HFL refer to LLCB during horizontal increment and vertical reset cycles.
12. Asynchronous signals. Its timing refers to the 1.5 V switching point of $\overline{VOE}$ input signal (pin 53).
13. The timing refers to the 1.5 V switching point of VMUX signal (pin 46) in 32- to 16-bit multiplexing mode. Corresponding pairs of VRO outputs are together connected.



(1) Related to VCLK (HFL).

Fig.31 Data output timing (VCLK).

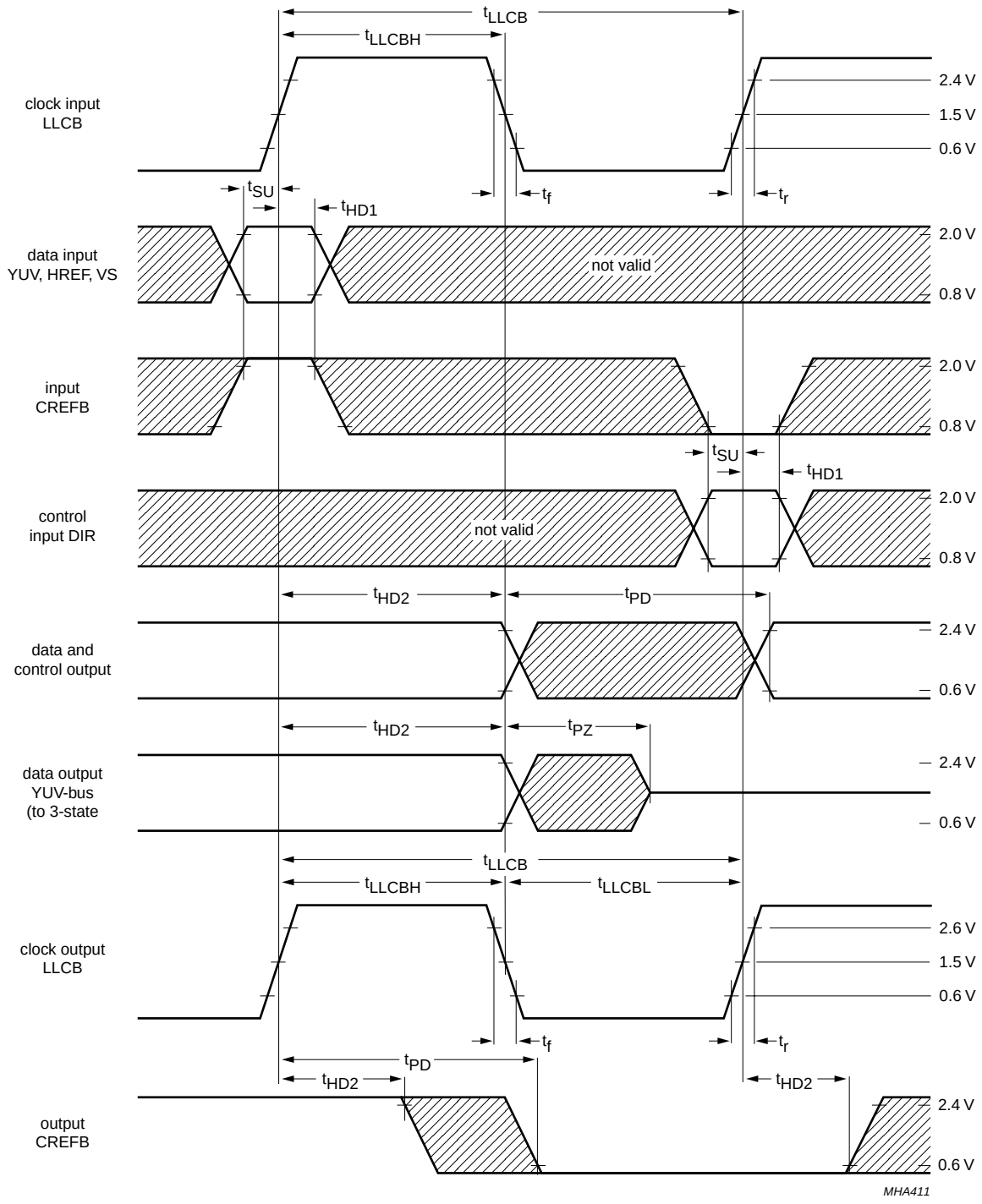


Fig.32 Data input/output timing by LLCB.

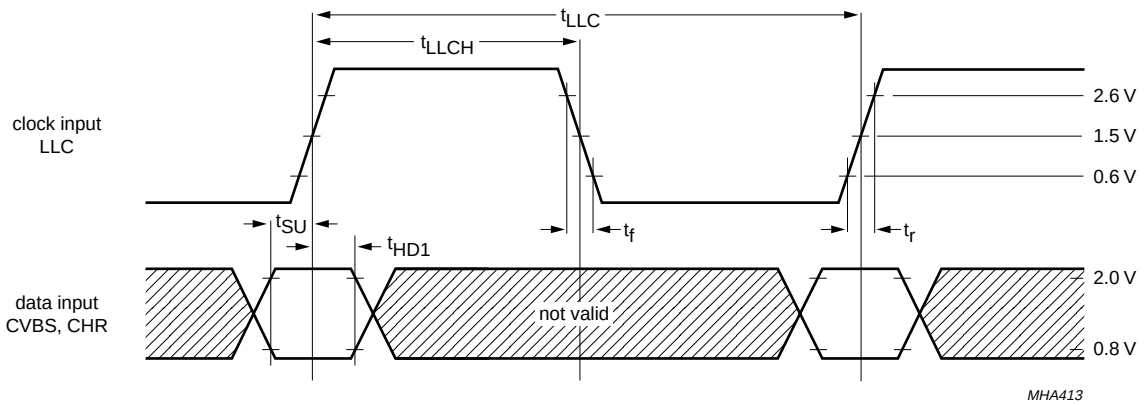
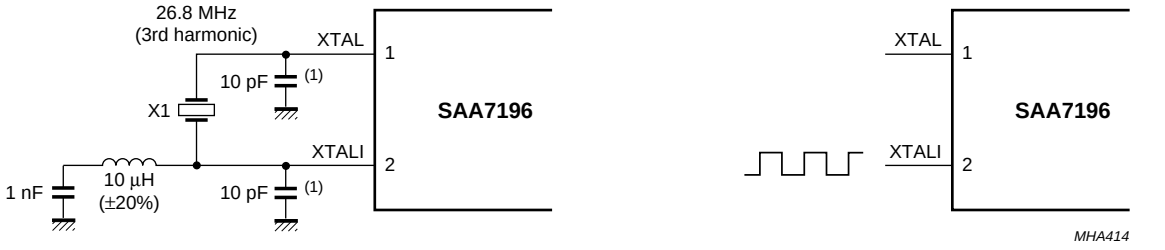


Fig.33 Data input timing by LLC.



a. Oscillator application.

b. Optional clock from external source.

(1) Value depends on crystal parameters.

Fig.34 Oscillator application circuits.

11 PROCESSING DELAYS

Table 37 Processing delays of signals

PORTS	DELAY IN LLC/LLCB CYCLES	REMARKS
CVBS/CHR to YUV	216	–
YUV to VRO	56 in YUV mode	only in transparent mode
	58 in RGB mode	only in transparent mode
CVBS/CHR to VRO	272 in YUV mode	only in transparent mode
	274 in RGB modes	only in transparent mode

12 APPLICATION INFORMATION

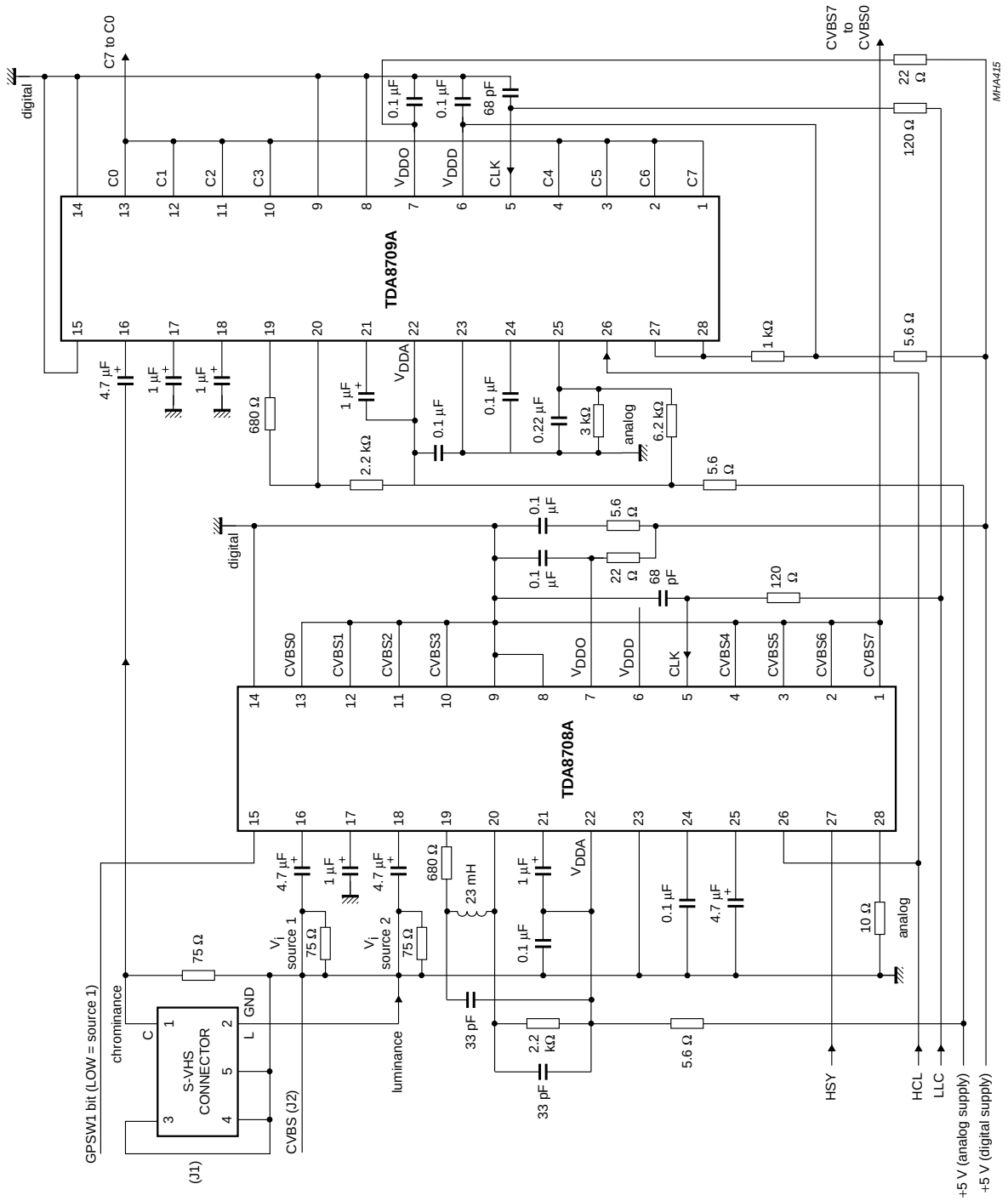


Fig.35 Application circuit analog-to-digital conversions.

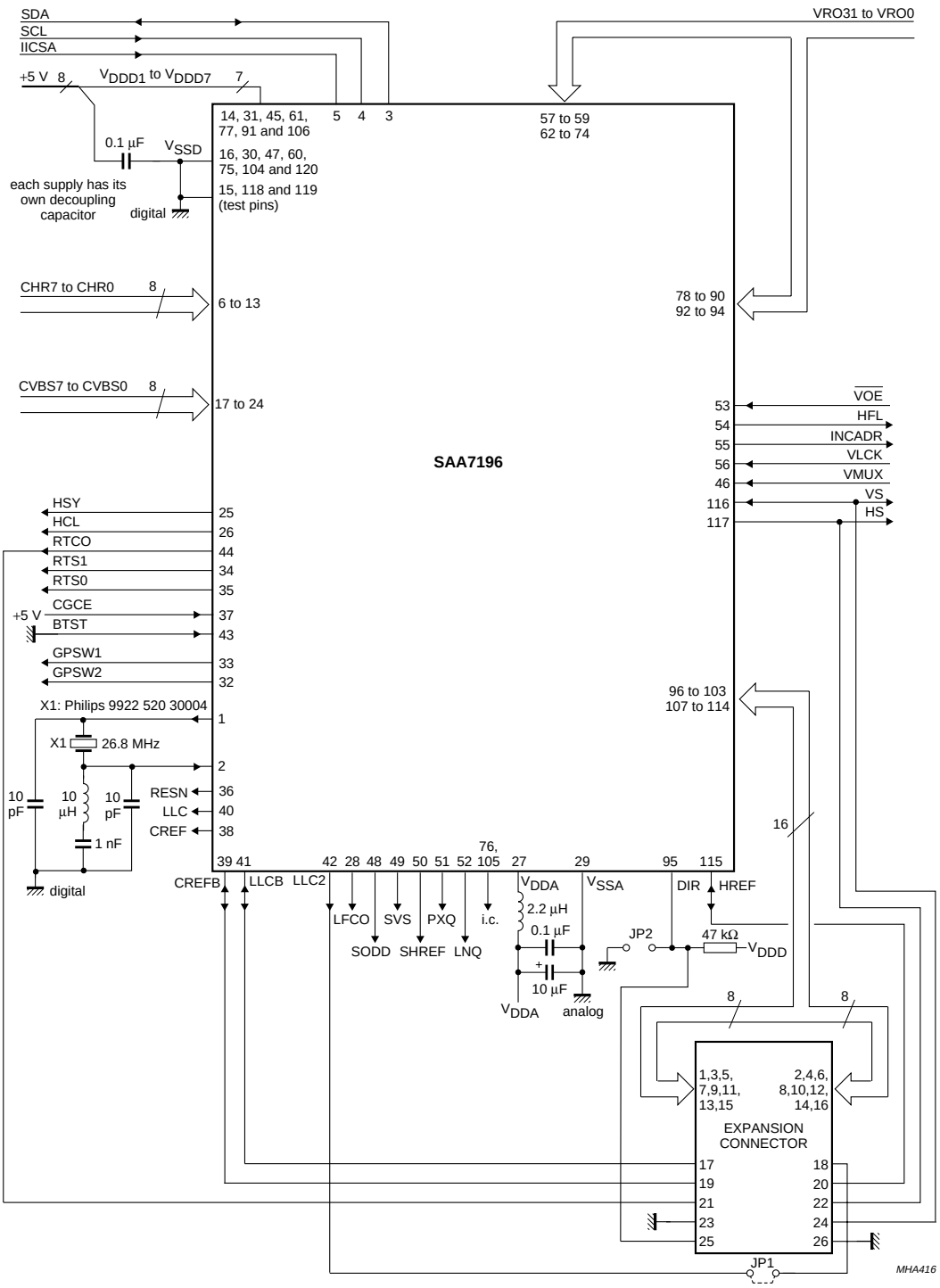


Fig.36 Application of SAA7196.

12.1 Programming example

Coefficients to set operation for application circuits Figs 35 and 36. Slave address byte is 40H at pin 5 connected to V_{SSD} (or 42H at pin 5 connected to V_{DDD}).

Table 38 Programming examples

SUBADDRESS	BITS	FUNCTION	VALUE (HEX)
00	IDEL7 to IDEL0	increment delay	4C
01	HSYB7 to HSYB0	H-sync beginning for 50 Hz	30
02	HSYS7 to HSYS0	H-sync stop for 50 Hz	00
03	HCLB7 to HCLB0	H-clamp beginning for 50 Hz	E8
04	HCLS7 to HCLS0	H-clamp stop for 50 Hz	B6
05	HPHI7 to HPHI0	HS pulse position for 50 Hz	F4
06	BYPS, PREF, BPSS1 and BPSS0, CORI1 and CORI0, APER1 and APER0	luminance bandwidth control	01(1)
07	HUEC7 to HUEC0	hue control (0 degree)	00
08	CKTQ4 to CKTQ0	colour-killer threshold QUAM	F8
09	CKTS4 to CKTS0	colour-killer threshold SECAM	F8
0A	PLSE7 to PLSE0	PAL-switch sensitivity	40
0B	SESE7 to SESE0	SECAM switch sensitivity	40
0C	COLO, LFIS1 and LFIS0	chrominance gain control settings	00
0D	VTRC, RTSE, HRMV, SSTB, SECS	standard/mode control	04(2)(3); 05(4)(3)
0E	HPLL, OECL, OEHV, OEYC, CHRS, GPSW2 and GPSW1	I/O and clock controls	38, 3B(5)
0F	AUFD, FSEL, SXCR, SCEN, YDEL2 to YDEL0	miscellaneous controls #1	90
10	HRFS, VNOI1 and VNOI0	miscellaneous controls #2	00
11	CHCV7 to CHCV0	chrominance gain nominal value	2C(6); 59(7)
12	SATN6 to SATN0	chrominance saturation control value	40
13	CONT6 to CONT0	luminance contrast control value	40
14	HS6B7 to HS6B0	H-sync beginning for 60 Hz	34
15	HS6S7 to HS6S0	H-sync stop for 60 Hz	0A
16	HC6B7 to HC6B0	H-clamp beginning for 60 Hz	F4
17	HC6S7 to HC6S0	H-clamp stop for 60 Hz	CE
18	HP6I7 to HP6I0	HS pulse position for 60 Hz	F4
19	BRIG7 to BRIG0	luminance brightness control value	80
1A to 1F	reserved	set to zero	00
20	RTB, OF1 and OF0, VPE, LW1 and LW0, FS1 and FS0	data formats and field sequence processing	10(8)
21	XD7 to XD0	LSBs output pixel/line	80(9); FF(10)
22	XS7 to XS0	LSBs input pixel/line	80(9); FF(10)

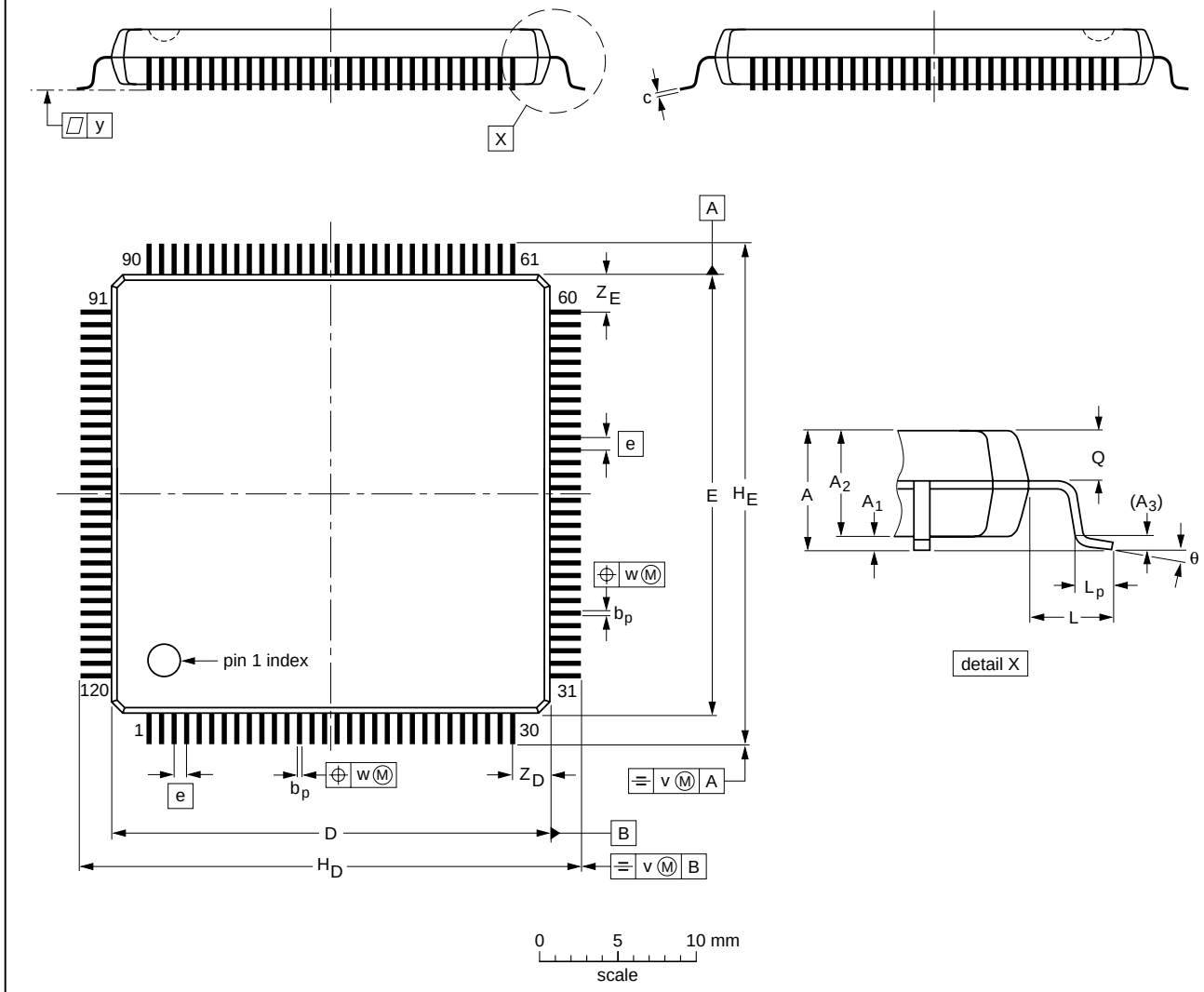
SUBADDRESS	BITS	FUNCTION	VALUE (HEX)
23	XO7 to XO0	LSBs for horizontal window start position	03[9]; 00[10]
24	HF2 to HF0, XO8, XS8 and XS9, XD8 and XD9	horizontal filter select and MSBs of subaddresses 21, 22, 32	85[9]; 8F[10]
25	YD7 to YD0	LSBs output lines/field	90[9]; FF[10]
26	YS7 to YS0	LSBs input lines/field	90[9]; FF[10]
27	YO7 to YO0	LSBs vertical window start position	03[9]; 00[10]
28	AFS, VP1 and VP0, YO8, YS8 and YS9, YD8 and YD9	MSBs of subaddresses 25, 26, 27	00[9]; 0F[10]
29	VS7 to VS0	LSBs vertical bypass start position	00[11]
2A	VC7 to VC0	LSBs vertical bypass lines/field	00[11]
2B	VS8,VC8, POE	MSBs of subaddresses 29, 2A and odd/even polarity switch	00[11]
2C	VL7 to VL0	chroma key: lower limit V (R–Y)	00
2D	VU7 to VU0	chroma key: upper limit V (R–Y)	FF[12]
2E	UL7 to UL0	chroma key: lower limit U (B–Y)	00
2F	UU7 to UU0	chroma key: upper limit U (B–Y)	00
30	VOF, AFG	VRAM port MUX enable, adaptively	80[13]

Notes

1. Dependent on application (Figs 35 and 36).
2. For QUAM standards.
3. HPLL is in TV-mode, value for VCR-mode is 84H (85H for SECAM VCR-mode).
4. For SECAM.
5. For Y/C-mode.
6. Nominal value for UV-CCIR-level with NTSC source.
7. Nominal value for UV-CCIR-level with PAL source.
8. ROM-table is active, scaler processes both fields for interlaced display; VRAM port enabled; long word position = 0; 16-bit 4 : 2 : 2 YUV output format selected.
9. Scaler processes a segment of (384 pixels $\times$ 144 lines) with defaults XO and YO set to the first valid pixel/line and line/field (for decoder as input source) with scaler factors of 1 : 1; horizontal and vertical filters are bypassed, filter select adaptability is disabled.
10. If no scaling and panning is wanted, the parameters XD, XS, YD and YS should be set to maximum (3FFH) and the parameters XO and YO should be set to minimum (000H). In this case, the HREF and VS signals define the processing window of the scaler.
11. No vertical bypass region is defined.
12. Chrominance keyer is disabled (VL = 0, VU = –1).
13. 32-bit to 16 VRAM port MUX, adaptive scale and Y-limiter are disabled; pixel and line qualifier polarity for transparent mode are set to zero (active); data burst transfer for the 32-bit long word formats is set.

13 PACKAGE OUTLINE

QFP120: plastic quad flat package;
120 leads (lead length 1.95 mm); body 28 x 28 x 3.4 mm; high stand-off height **SOT349-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.95	0.40 0.25	3.70 3.15	0.25	0.45 0.30	0.23 0.13	28.1 27.9	28.1 27.9	0.8	32.2 31.6	32.2 31.6	1.95	1.1 0.7	1.70 1.55	0.3	0.2	0.1	2.6 2.2	2.6 2.2	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT349-1						~~93-08-25~~ 95-02-04

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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